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Enabling High-Speed Die-to-Die Interfaces with Wallstrip: A Study on Insertion Loss and Crosstalk Metrics with a Novel Transmission Line Structure

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SPEAKERS

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Stephen Newberry received his B.S. degree in electrical and computer engineering (ECE) from Rutgers University, New Brunswick, NJ, USA in 2015 and his M.S. degree in electrical engineering (EE) from the University of Idaho, Moscow, ID, USA in 2024. Prior to his B.S. degree, he was an Electrician's Mate with the U.S. Coast Guard. He has held various roles in hardware design and signal integrity engineering, most recently as a Signal and Power Integrity Engineer at Chipletz

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Victor Kronberg is an electrical engineer specializing in IC package design. He holds a master's degree in electrical & computer engineering (ECE) from the University of Colorado Boulder (2021) and multiple bachelor's degrees from the University of Texas at Austin (2014). Prior to joining Chipletz as an IC package design engineer, he was a field applications engineer at Siemens EDA (formerly Mentor Graphics)

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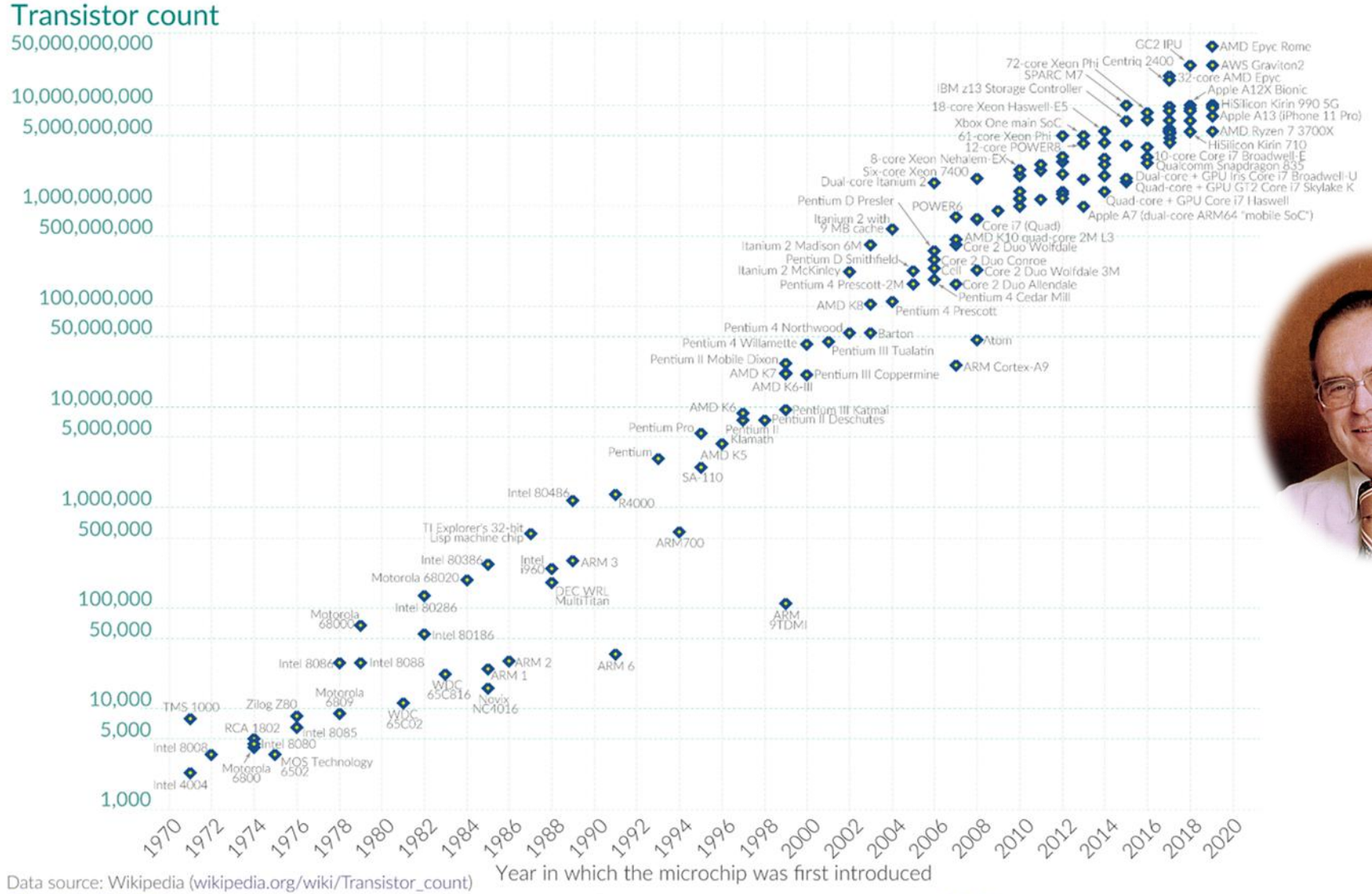
Ching-Ping Wong earned his Master of Science degree in Electrical Engineering at Mississippi State University in 1996. He started his career at Intel in RTL design engineering; then detoured into MCM package layout engineering at AIC Microelectronics before returning to Intel as I/O transistor-level circuit designer. He then worked as a microprocessor circuit designer during the height of the dot-com era at Santa Clara, California before returning as an I/O circuit designer and signal integrity engineer at Broadcom in 2002. He is currently with Chipletz, Inc, as Fellow Engineer in Signal and Power Integrity Engineering, since incorporated in 2021

Moore's Law: The number of transistors on microchips doubles every two years

Our World in Data

Moore's law describes the empirical regularity that the number of transistors on integrated circuits doubles approximately every two years. This advancement is important for other aspects of technological progress in computing – such as processing speed or the price of computers.

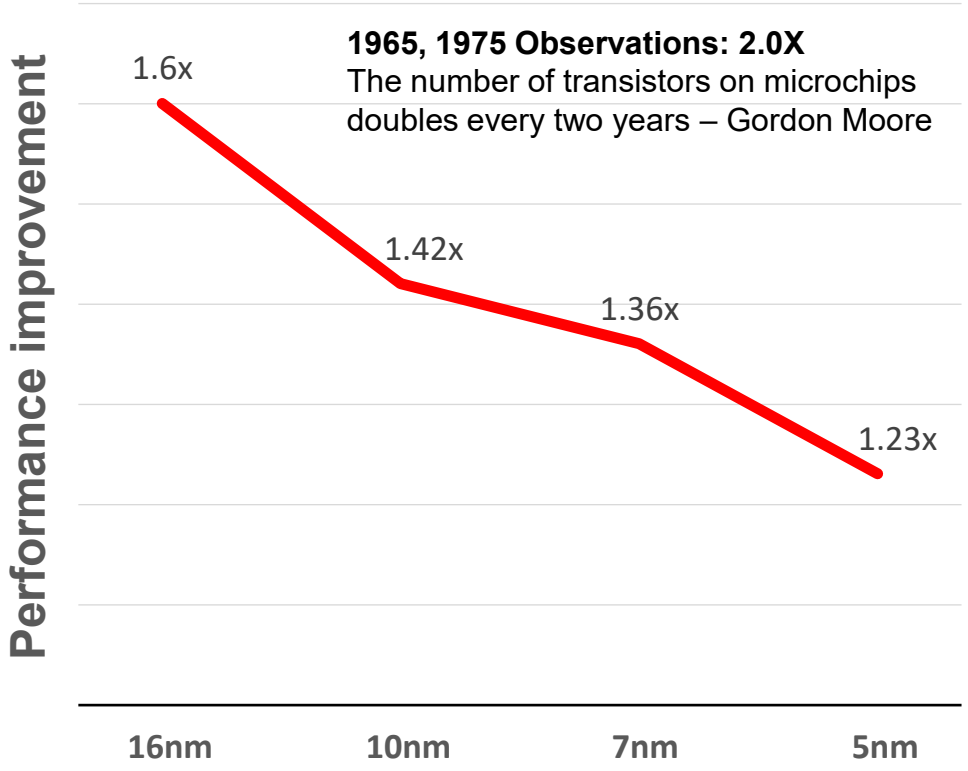


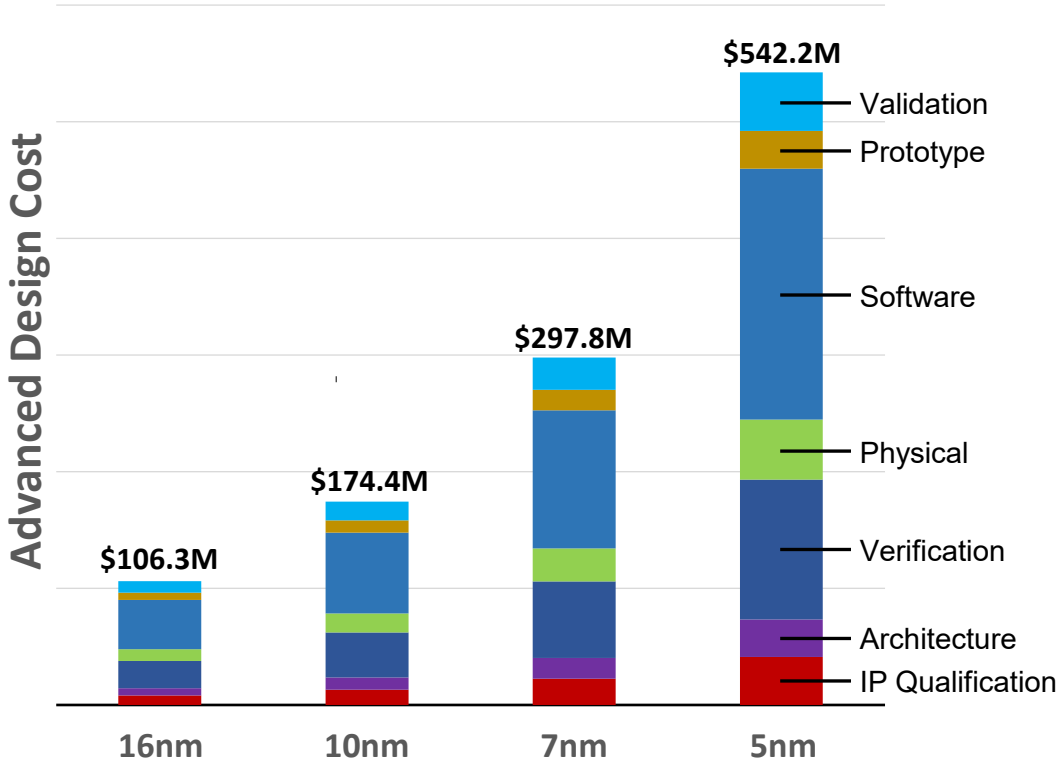
Data source: Wikipedia (wikipedia.org/wiki/Transistor_count)

OurWorldinData.org – Research and data to make progress against the world's largest problems.

Moore's Law Is Slowing Down

- Slowing of Moore's Law leads to less **performance improvement** for future nodes while **design cost** increases.
- Performance scaling will have to rely on silicon area growth leading to increased power consumption.
- Large high-performance compute system is best realized by **chiplet solutions**.





Source: IPS IEEE Heterogeneous Integration Roadmap

The High-Performance Compute System

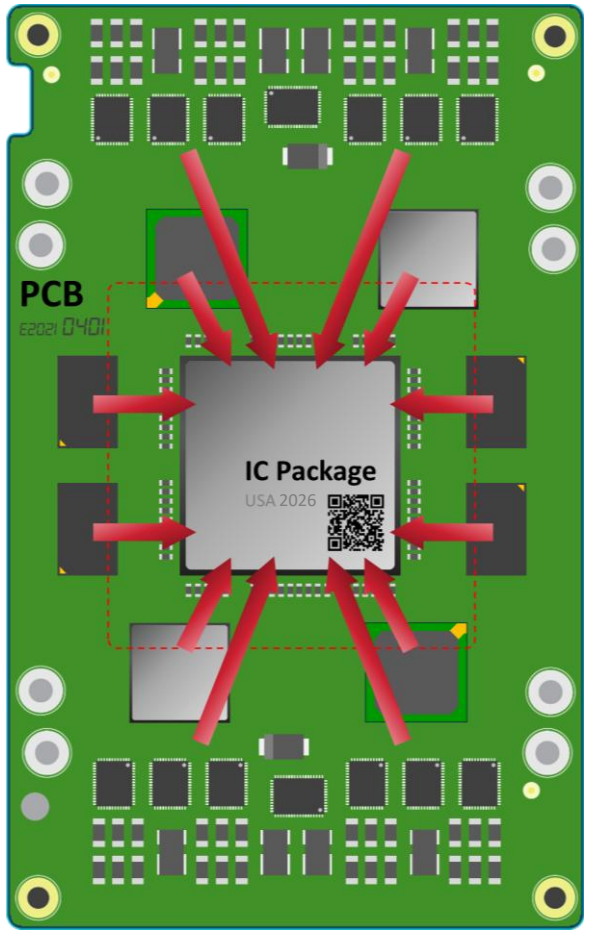
The system is integrating into the substrate

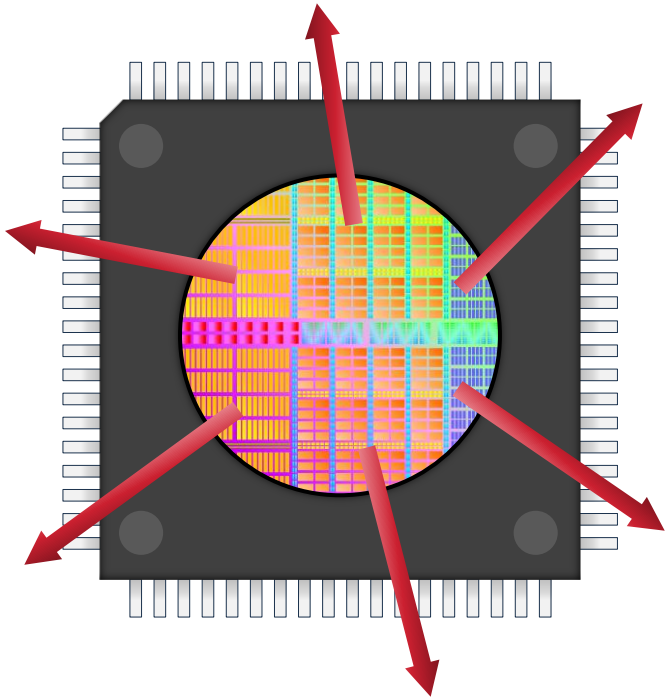
+

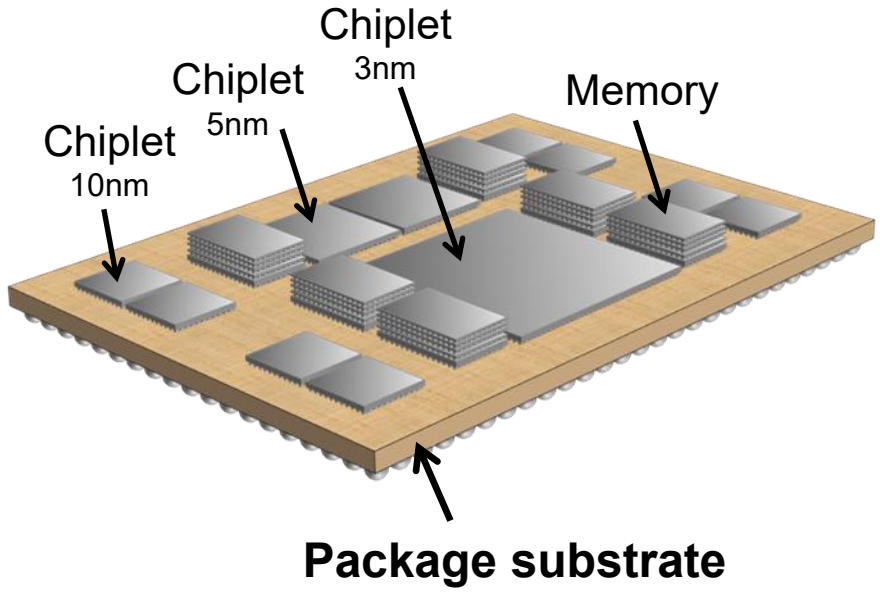
The SOC is disaggregating into the substrate

=

Lots of dies on a substrate

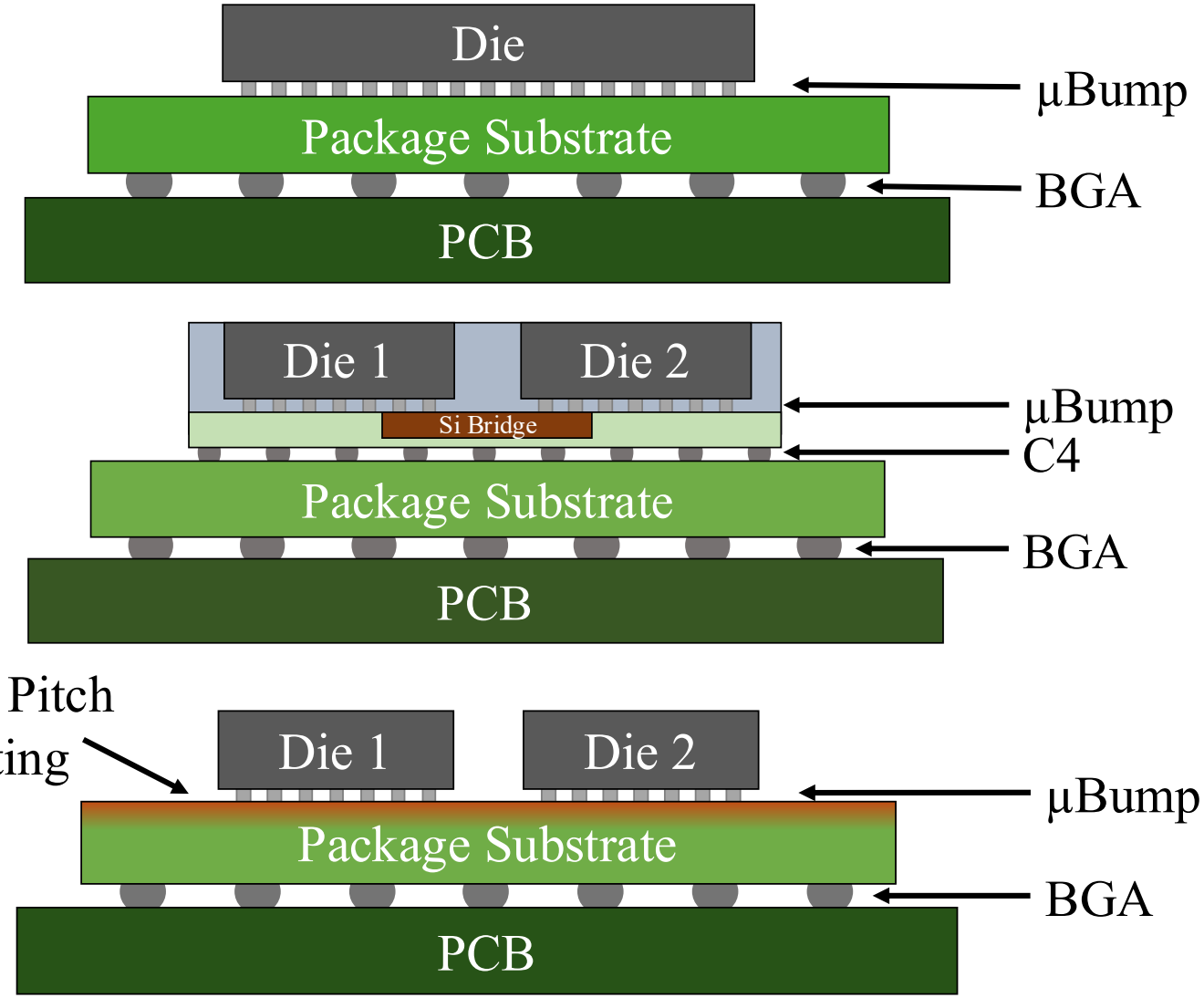






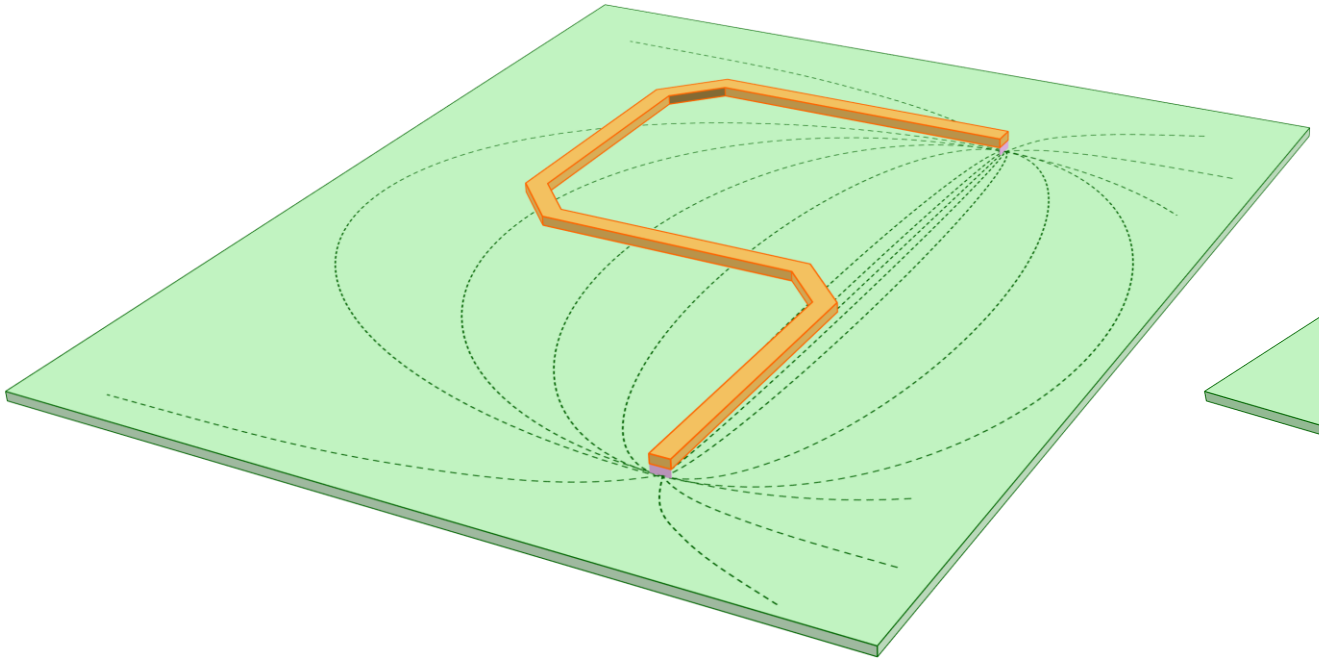
Chiplet Integration Architectures

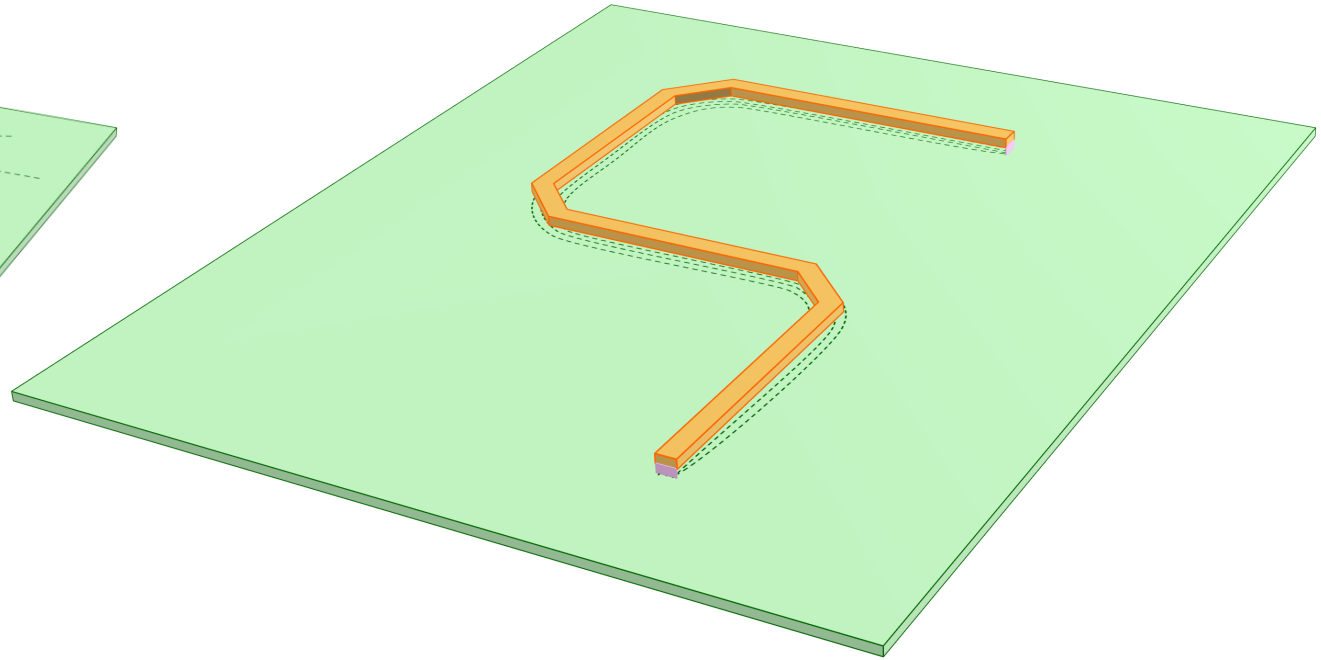
- Transition from monolithic (top) to chiplets on an interposer (middle) to chiplets directly on a package substrate without interposer (bottom)
- Monolithic:
  - Single process node for all functions
  - As die sizes increase, costs also increase and yield is reduced
- Chiplet on Interposer:
  - Enables heterogeneous process nodes
  - Reduces die size, improves yield
  - Adds additional C4 interface discontinuity
- Chiplet on Substrate
  - Maintains die size, yield
  - Eliminates interposer (cost reduced, C4 discontinuity removed)
  - Opportunity for improved die-to-die channel performance



Wallstrip Origins and Design Rules

Signal Return Path On The Microstrip



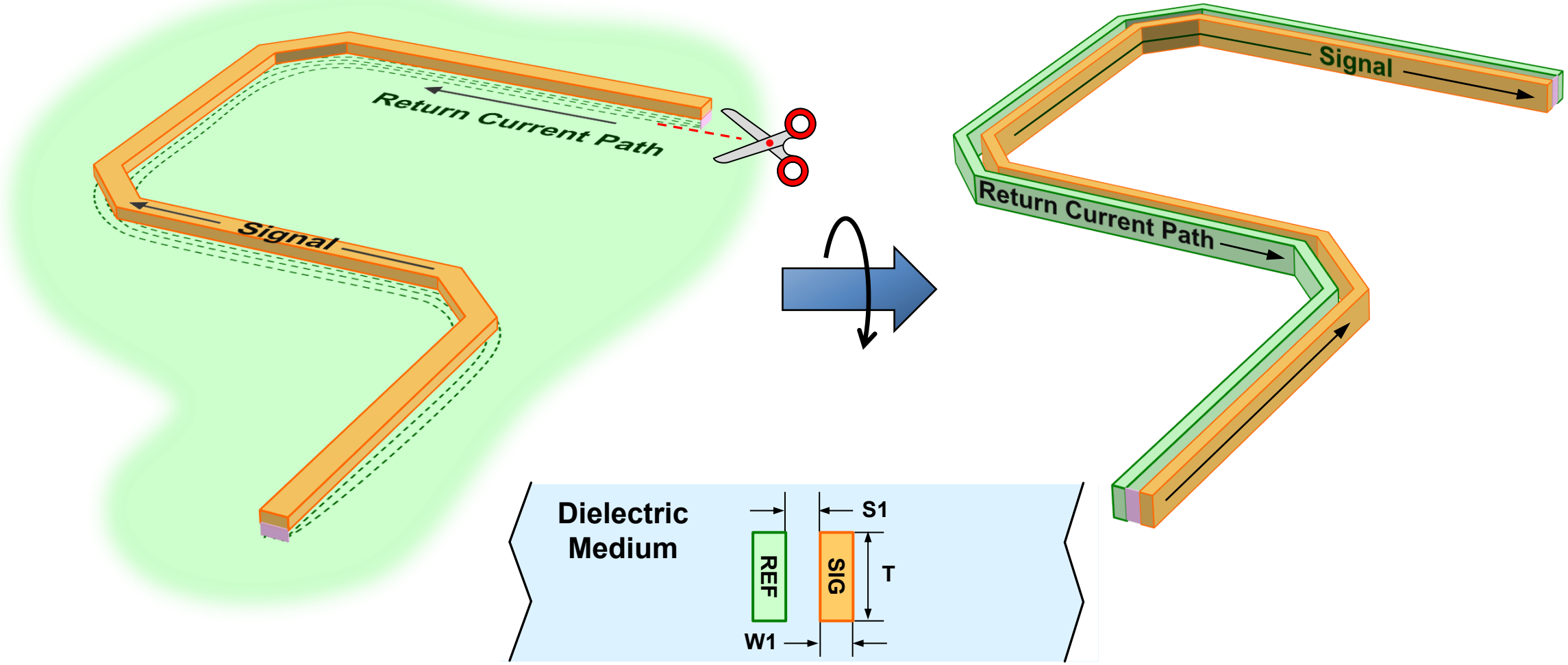


- Low speed return current path following least resistance.
- High speed return current path following least inductance.

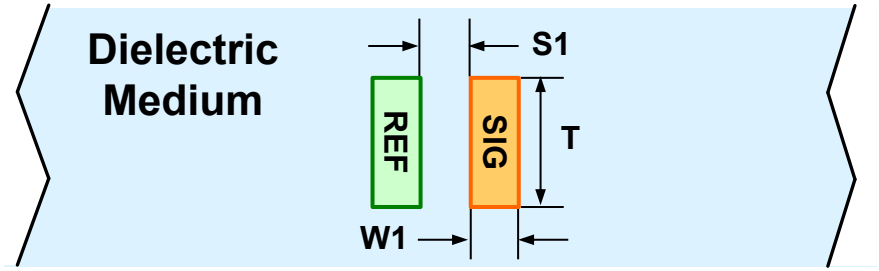
Reference:

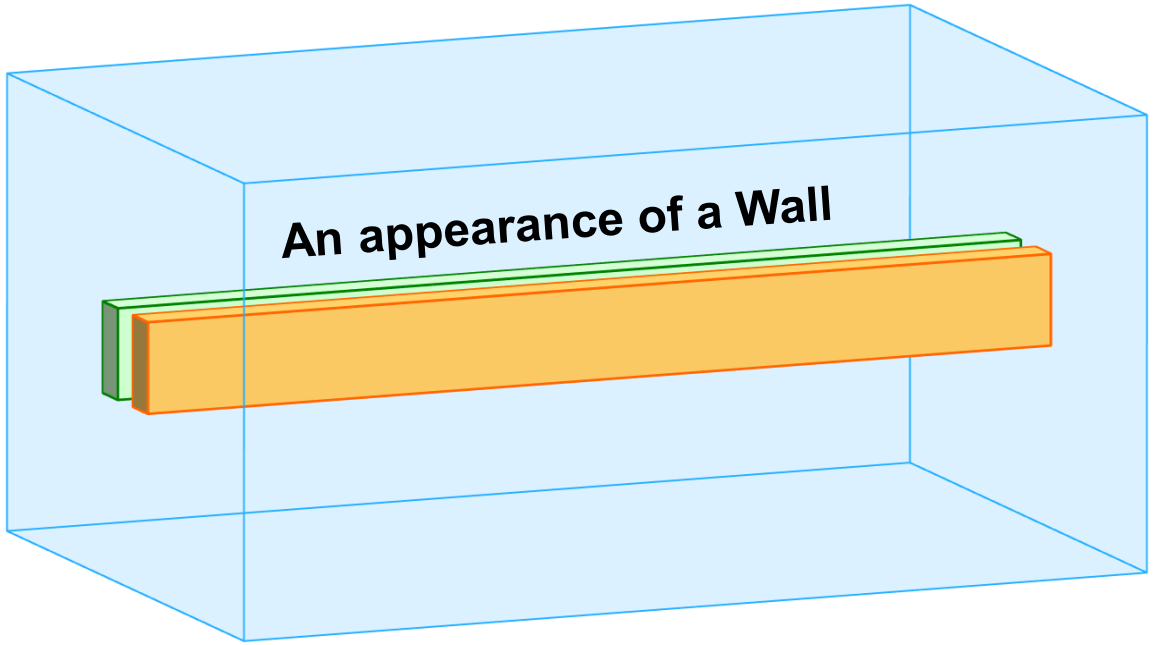
Howard Johnson and Martin Graham, High-Speed Digital Design – A Handbook Of Black Magic, 1st edition, Prentice Hall 1993

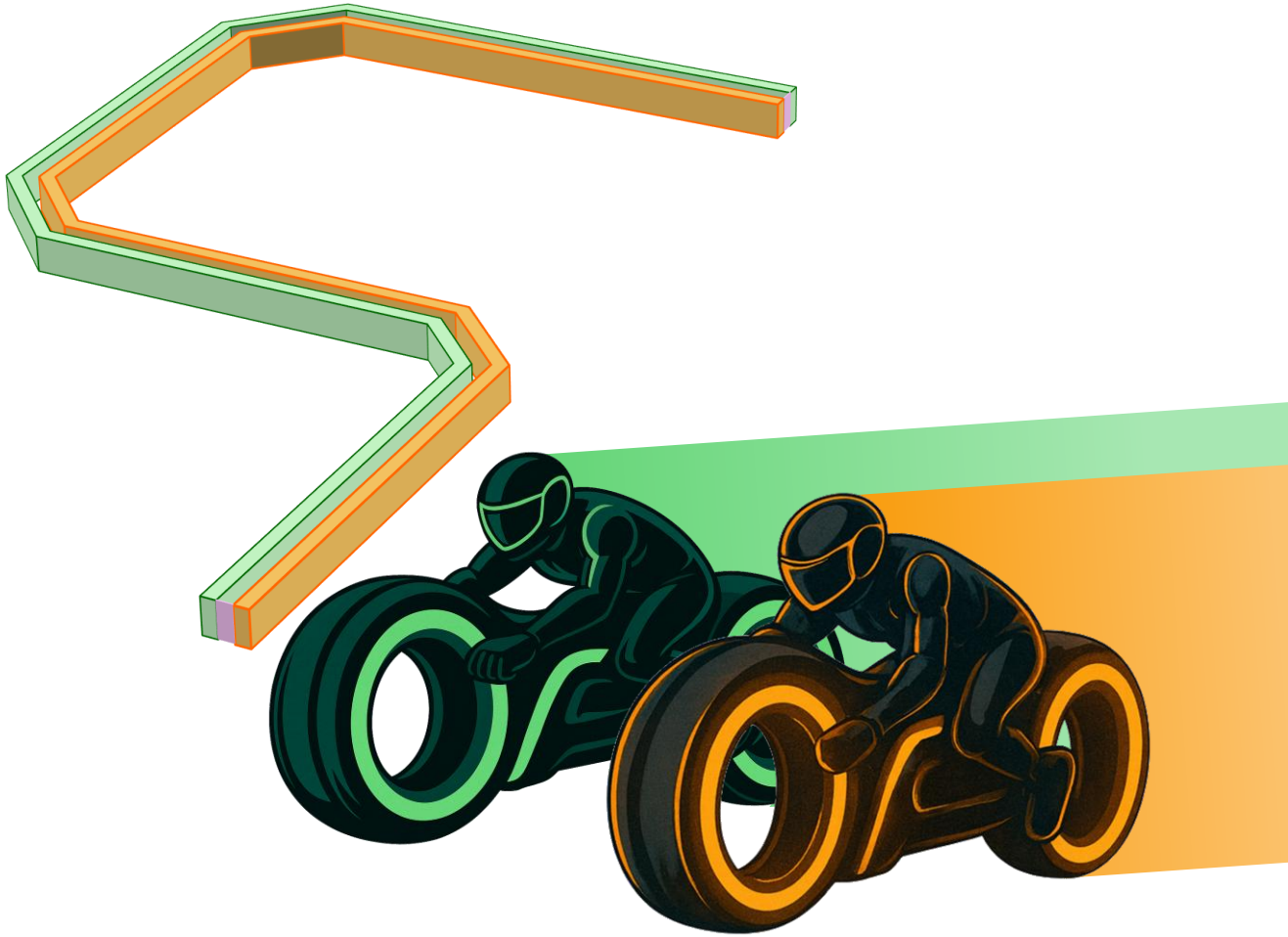
Microstrip Transformation



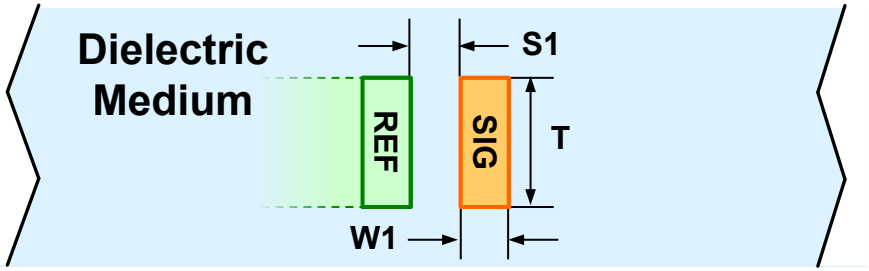
Wallstrip Transmission Line







Wallstrip Transmission Line

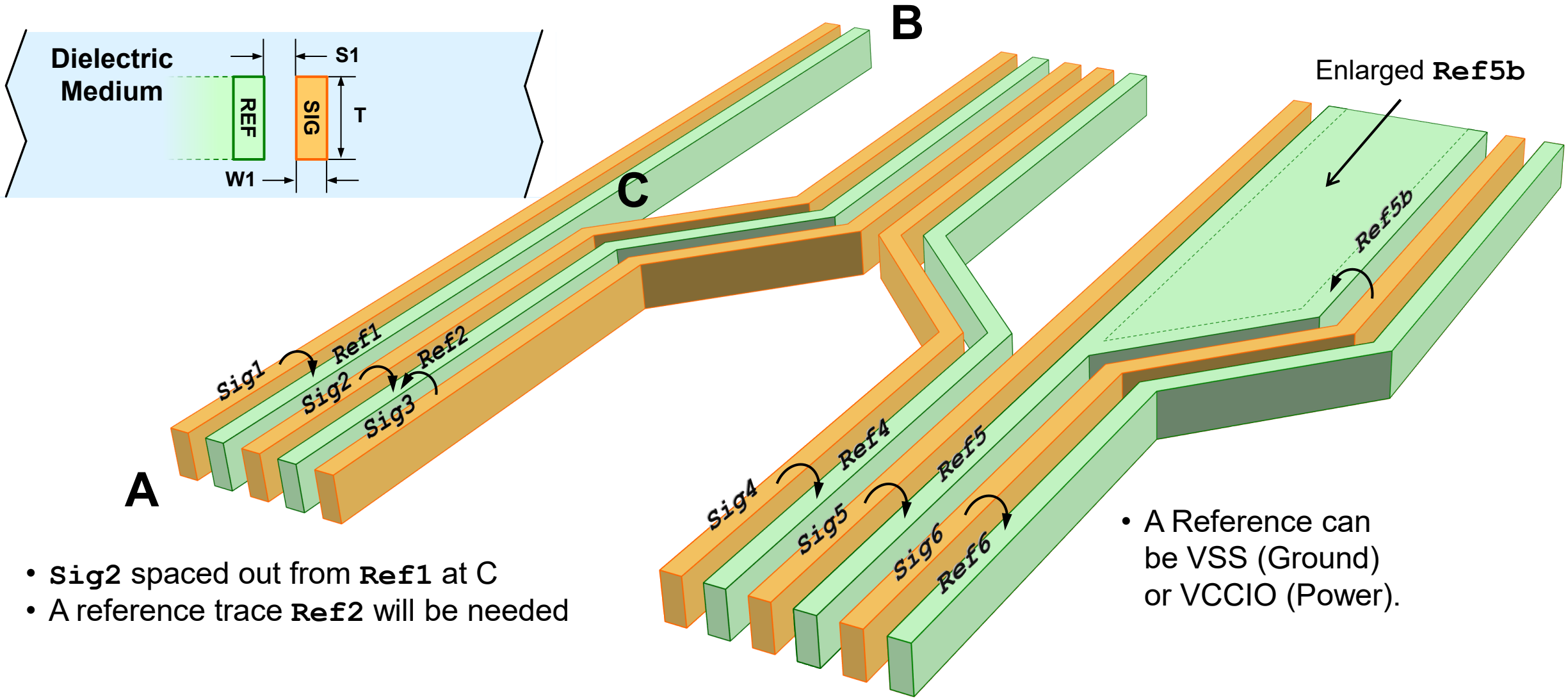


- Trace thickness T is ≥ 1.5x of signal width W1 including space S1, where the adjacent trace set as reference.
- At least 1 Reference trace will be needed.

- Wallstrip Reference trace can be enlarged at any path or wrapped around the Signal trace.

- Wallstrip space, **S1**, between Signal and Reference trace is to be kept constantly routed from Point **A** to **B**.

Wallstrip Transmission Line

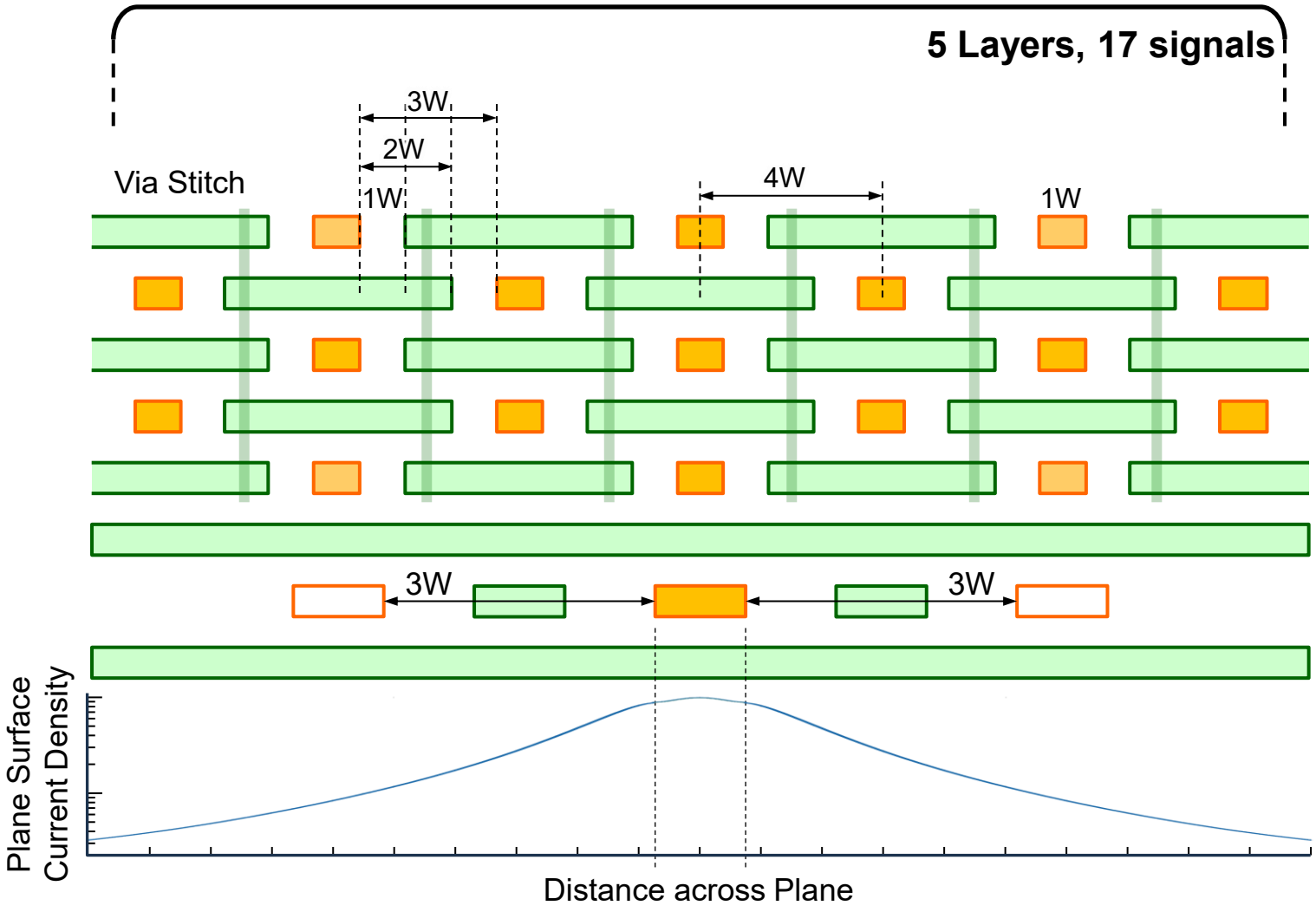


- **Sig2** spaced out from **Ref1** at C
- A reference trace **Ref2** will be needed

- A Reference can be VSS (Ground) or VCCIO (Power).

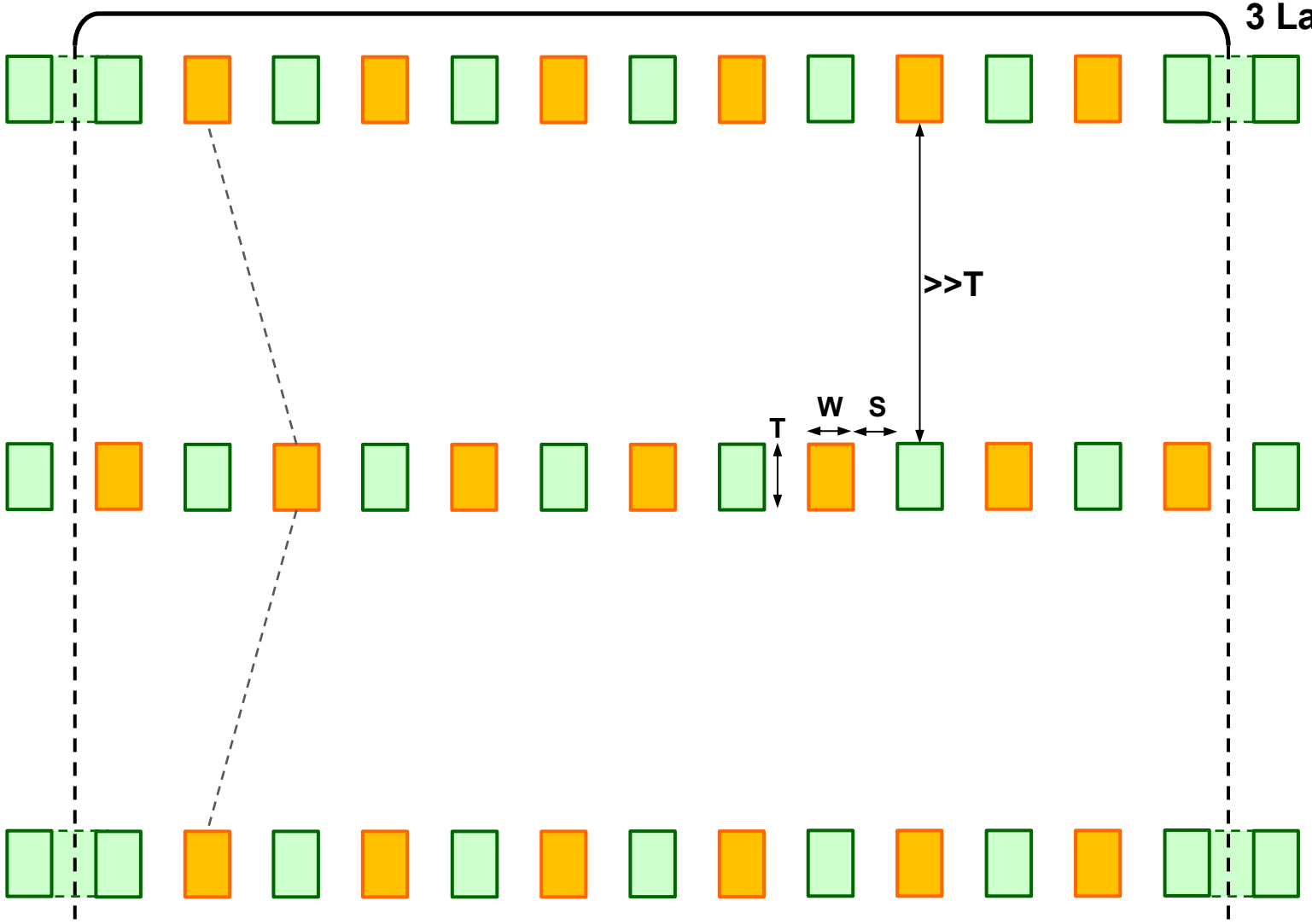
Package Layout with Wallstrip

A Stackup For Die-to-Die Connectivity



- Reference thoroughly covering the signal trace for crosstalk mitigation efforts.
- Signal trace is covered by at least 3 times the width by the pseudo reference plane.
  - Signal trace width reduction to accommodate high density routing.
  - Alternating signal and reference layers as an example.
  - Stackup for Die-to-Die (D2D) as shown.
- Return current density on reference plane as shown.
- For crosstalk mitigation, adjacent trace is best placed at least 3 times the width away.
- To further reduce crosstalk, additional trace is placed between the signals.

Chipletz Substrate Stackup Using Wallstrip



3 Layers, 19 signals

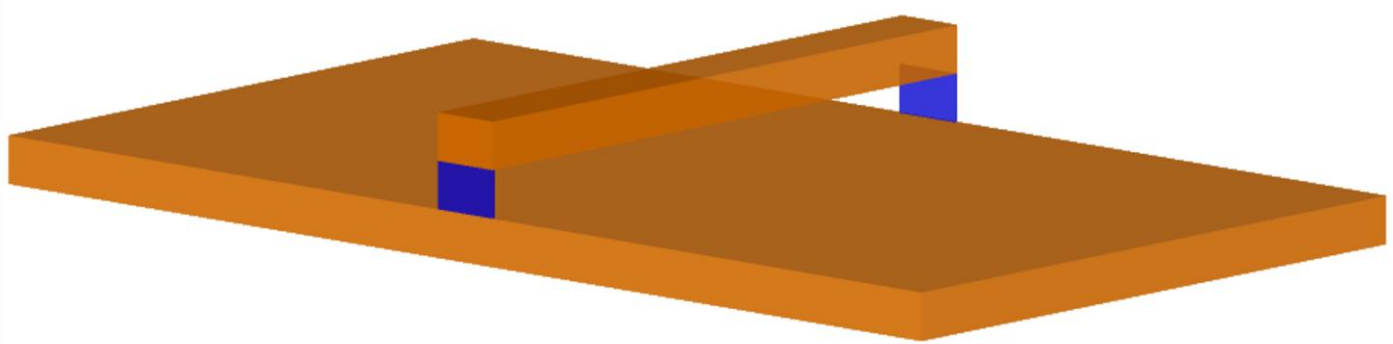
- Chipletz stackup metal to metal separation is significantly large in comparison to signal trace height, naturally reduce layer to layer crosstalk.
- Signals are offset horizontally for further crosstalk reduction.
- Reference traces re-allocated such that signal trace impedance and propagation delay are comparable to each other.
- Wallstrip traces are naturally taller.
- Stackup for D2D using Wallstrip transmission line as shown.
- Wallstrip traces do not require any reference plane placed either below or above its traces.

Channel Analysis with Wallstrip as Compared to Silicon Bridge

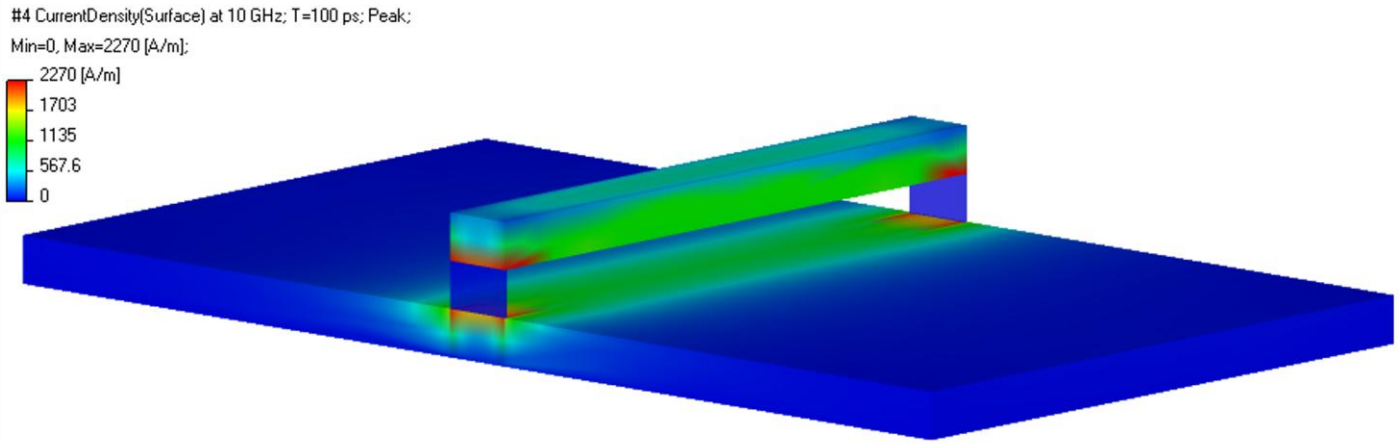
Developing Wallstrip: Microstrip Return Current

- Plot of current density in a microstrip at 10 GHz
- Return current is highly localized under the signal trace
- Much of the reference plane is electrically unused

(a)

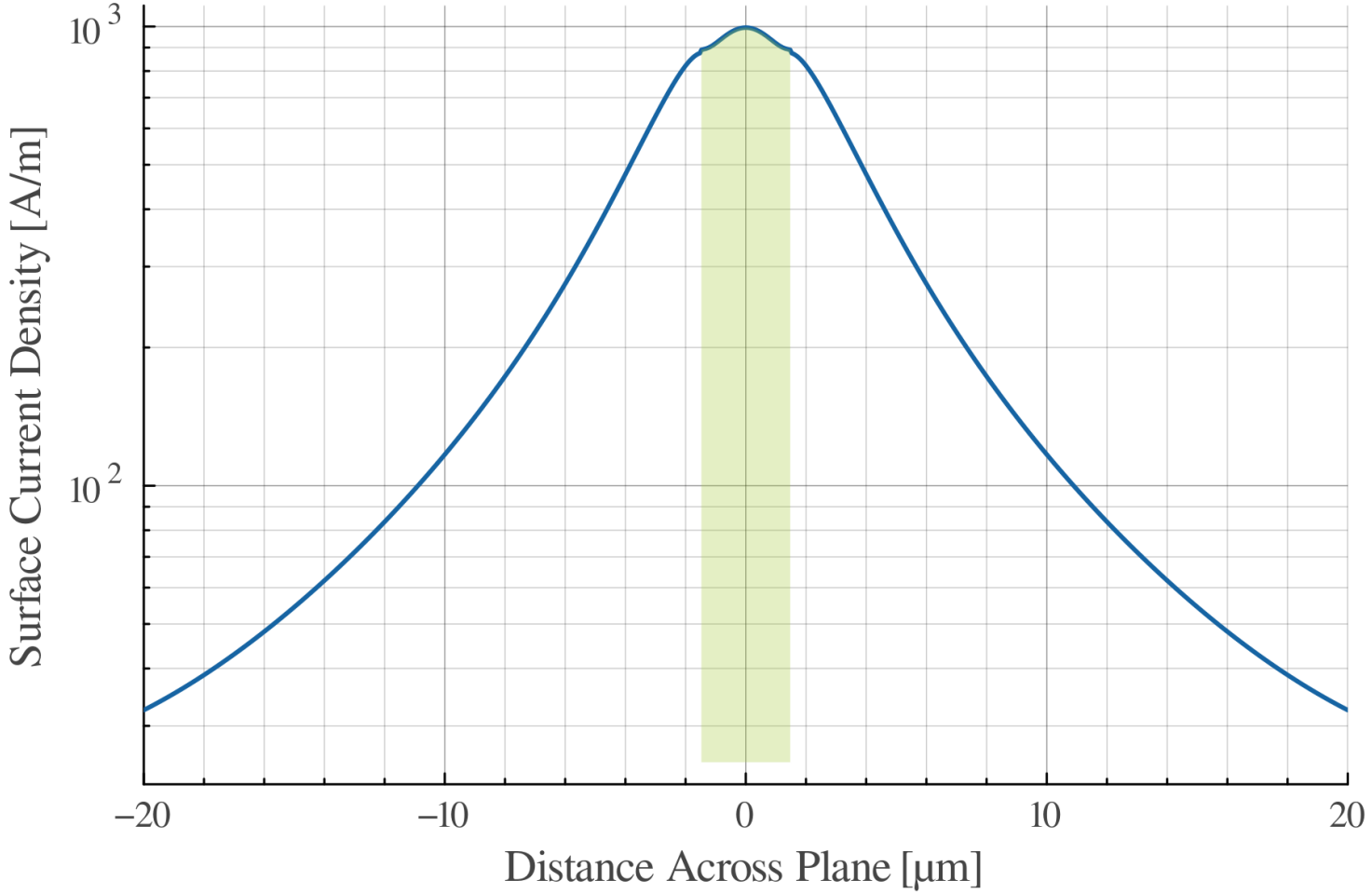


(b)



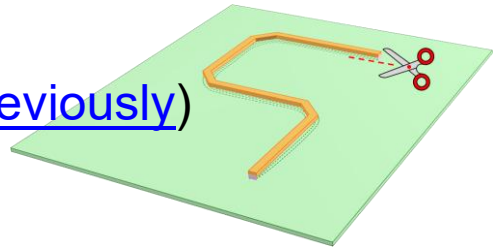
Developing Wallstrip: Microstrip Return Current

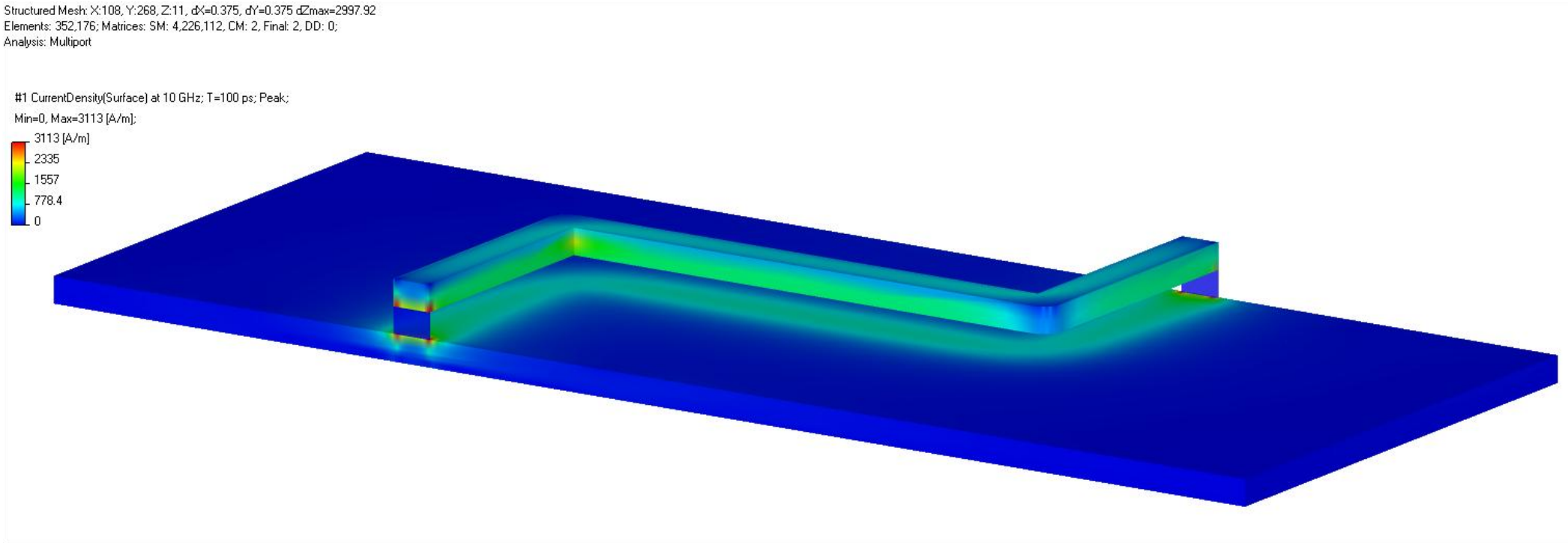
- The area of return path directly under the trace contains about 26% of the return current
- Cutting the return path will raise the characteristic impedance of the transmission line
  - 54.8Ω → 68.9Ω in this example
- Violates common rules-of-thumb about return plane width
  - Yet, this **enables** creation of Wallstrip topology



Developing Wallstrip: Microstrip Return Current

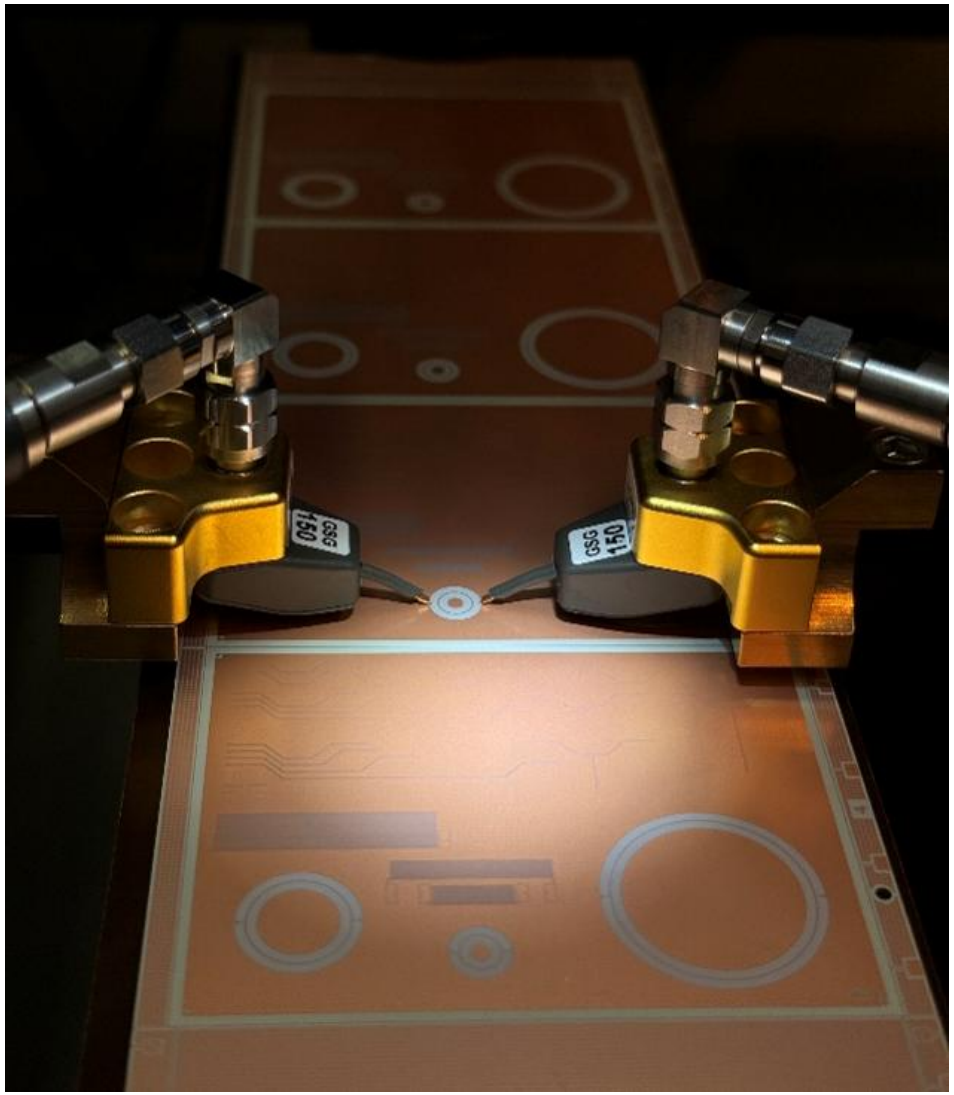
- Current follows return path in bend (as shown previously)
- Justification for cutting return path





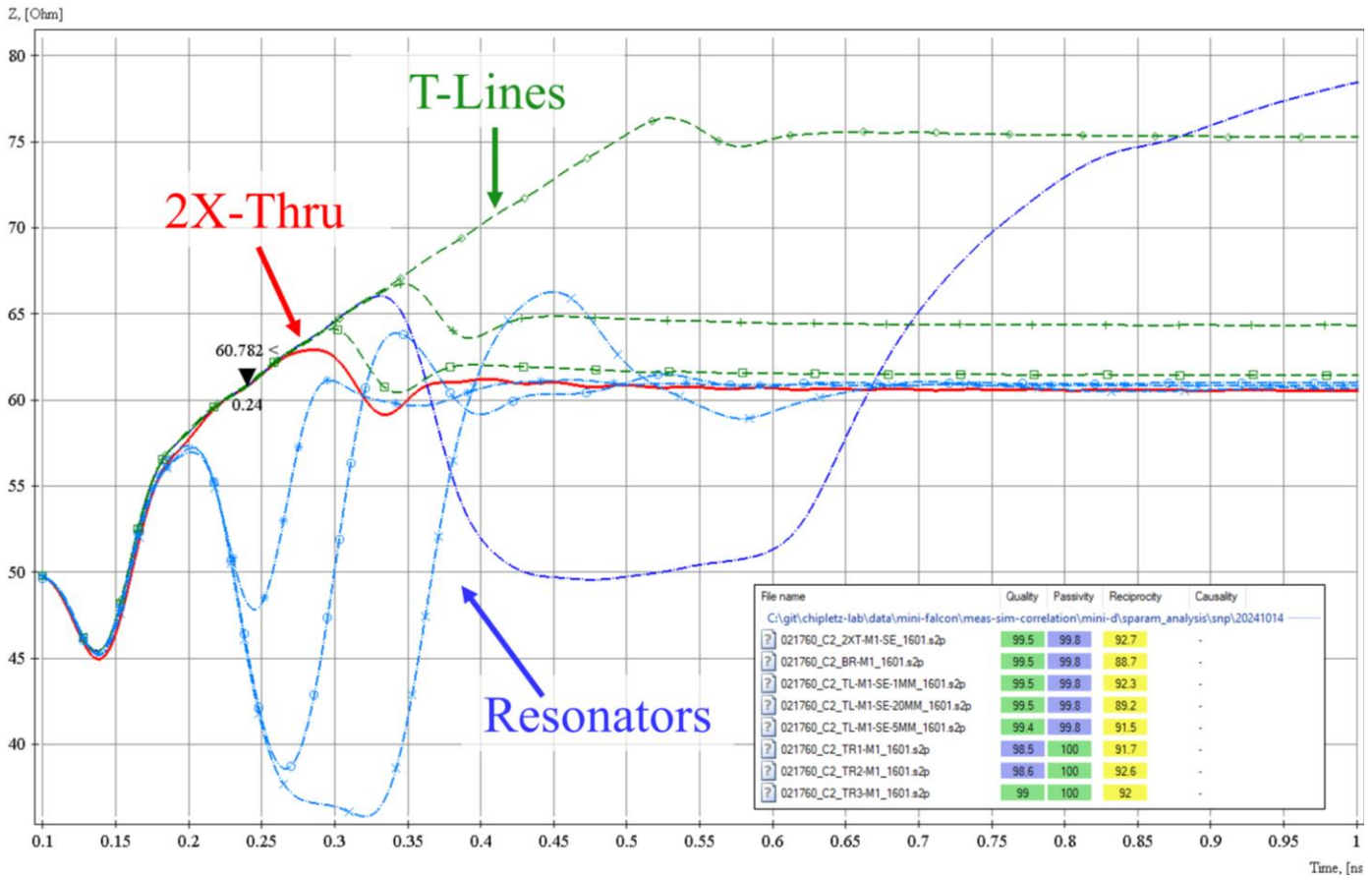
Material Property Identification

- Purpose
  - **Ensure simulation tool is adequate for small feature sizes**
  - **Optimize simulation tool configuration**
- Structures:
  - IEEE P370 2X-Thru
  - Single-ended and differential transmission lines
  - Beatty resonator
  - DC resistance measurement
- Minor material differences from expected final design configuration



2X-Thru Quality

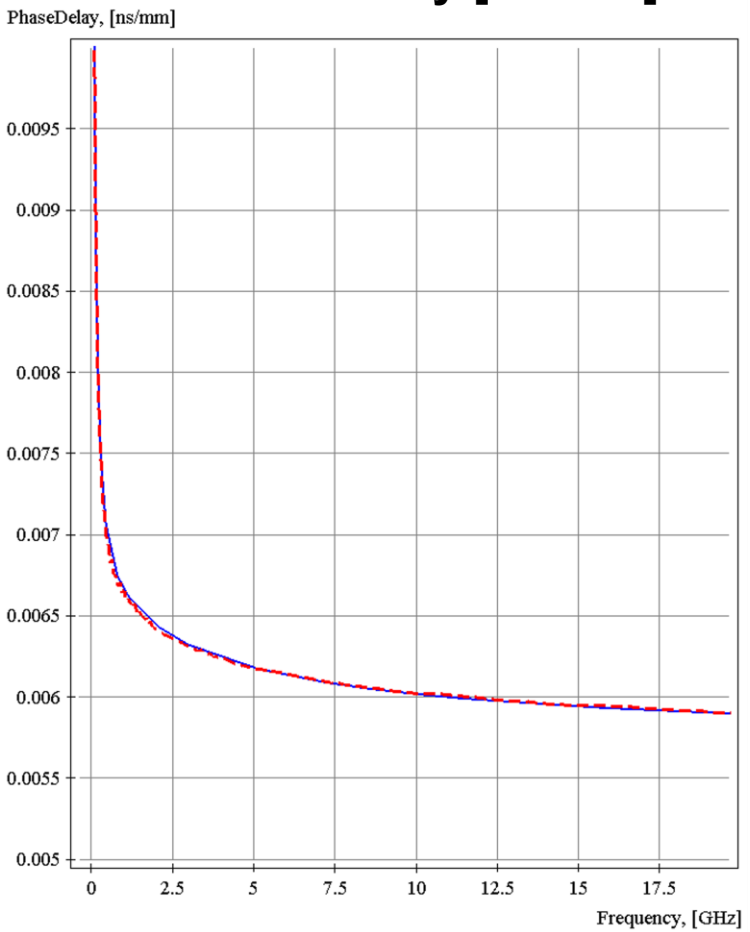
- Validated against IEEE P370 requirements
- TDR (at right) shows deviation of lead-in traces for structures compared to 2X-Thru
  - 0.19% worst-case deviation
  - Well within Class A limit of 2.5%
- Other fixture electrical requirements:
  - IL is Class A up to 20 GHz
  - RL is Class B up to 15 GHz
- Confirms fixture design and measurement quality prior to property extraction



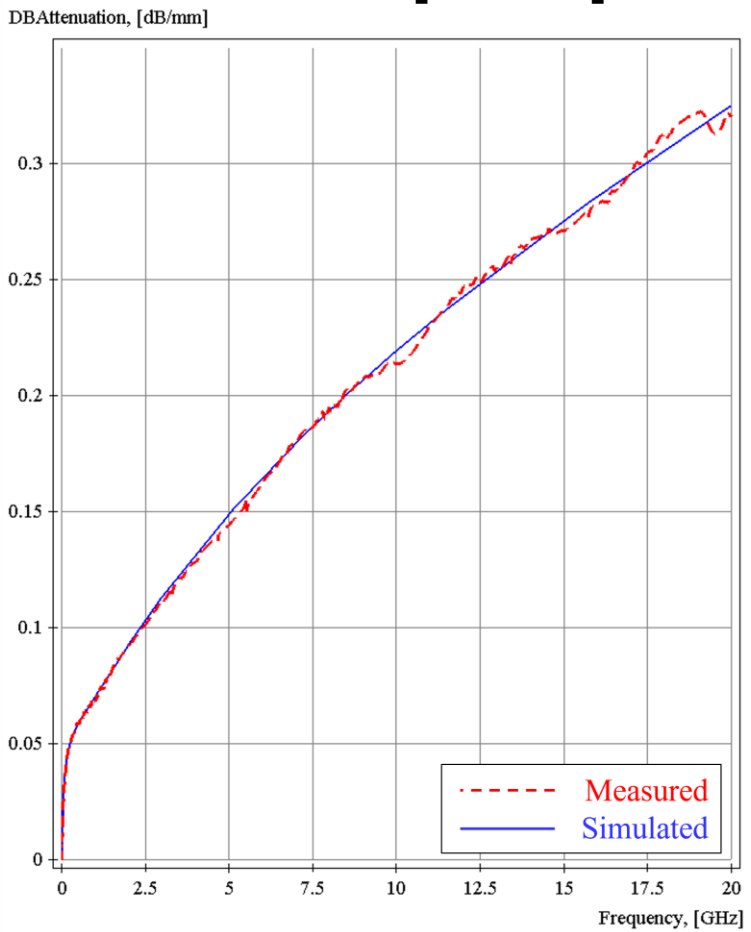
Extracted Material Properties

- Utilize Generalized Modal S-Parameter (GMS) method
- Iteratively tune simulation configuration and material property settings to match phase delay and attenuation
- **Provides confidence that Wallstrip simulations are valid**

Phase Delay [ns/mm]

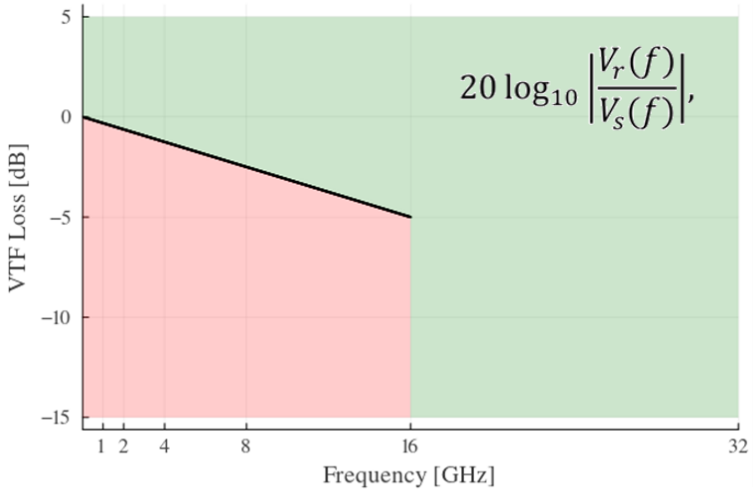


Attenuation [dB/mm]

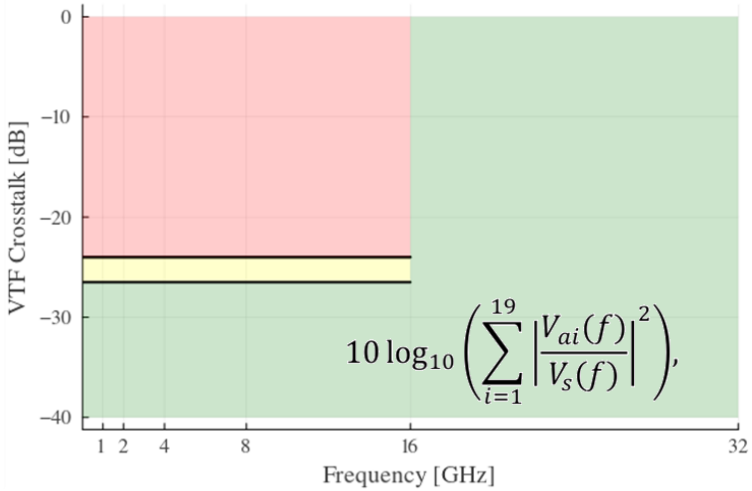


UCIe Performance Metrics

- UCIe: Universal Chiplet Interconnect Express
  - On-package, die-to-die interconnect standard
  - Varying cost/complexity options.
    - *All work here is with the Advanced Package*
- UCIe frequency domain metric:
  - Voltage Transfer Function (VTF)
  - Similar to S-Parameters
  - Masks shown at right
- VTF Loss:
  - 5 dB limit at Nyquist
  - 0 dB depends on Rx termination
  - This work is all unterminated at Rx
- VTF XT:
  - Use 19 aggressor signals
  - -24 dB limit in power-sum calculation
- Channel Eye Masks
  - 0.65UI/40mV rectangle for ≤ 32 Gbps
  - 0.65UI/65mV diamond for > 32 Gbps

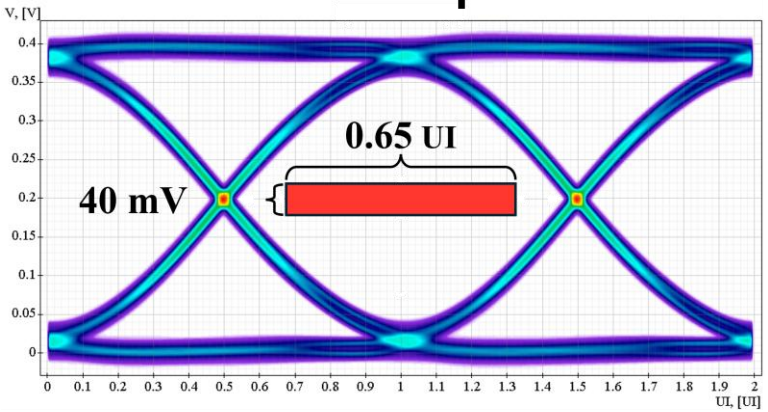


(a)



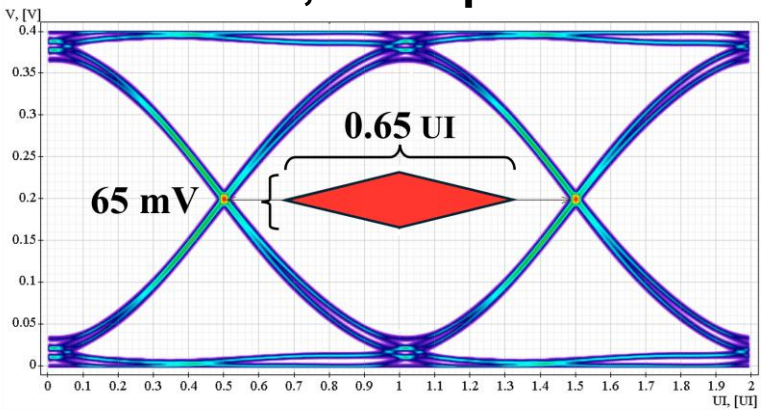
(b)

≤ 32 Gbps



(a)

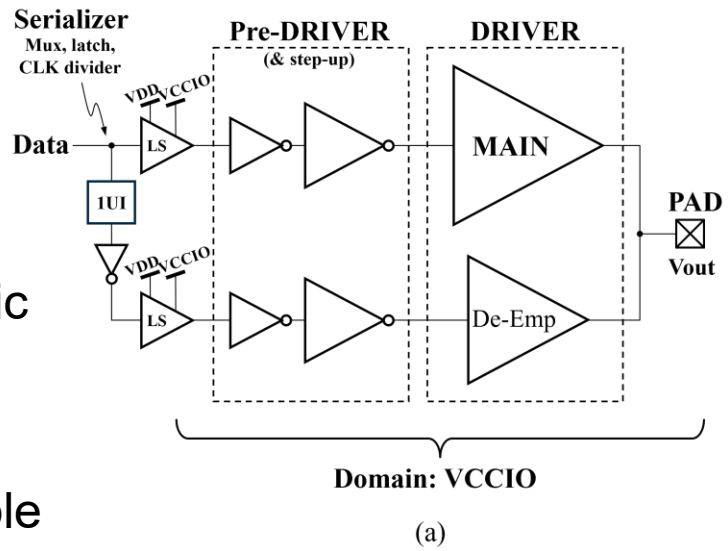
48, 64 Gbps

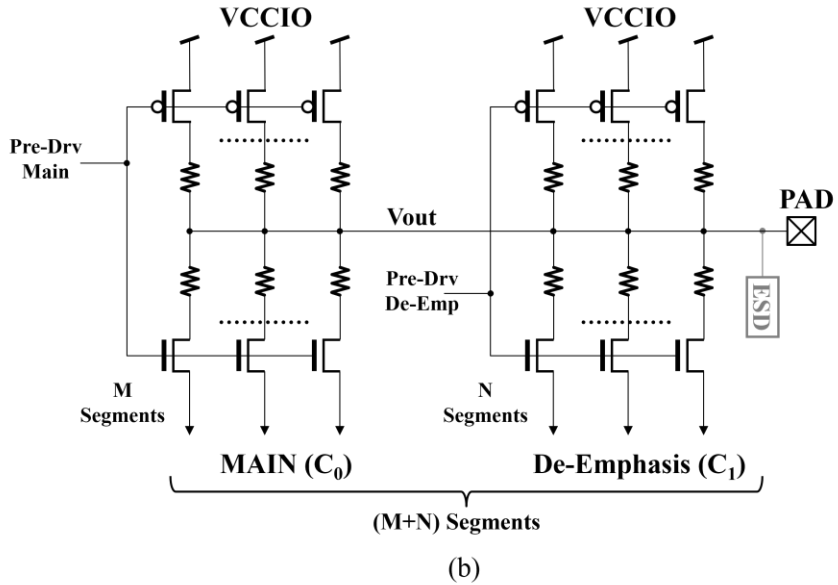


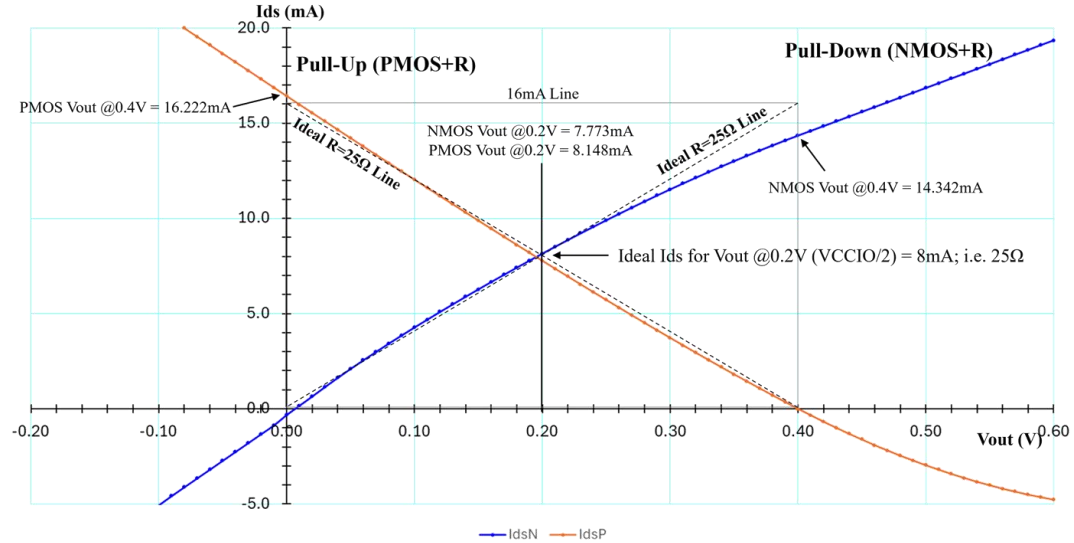
(b)

Custom UCIe Transmitter Model

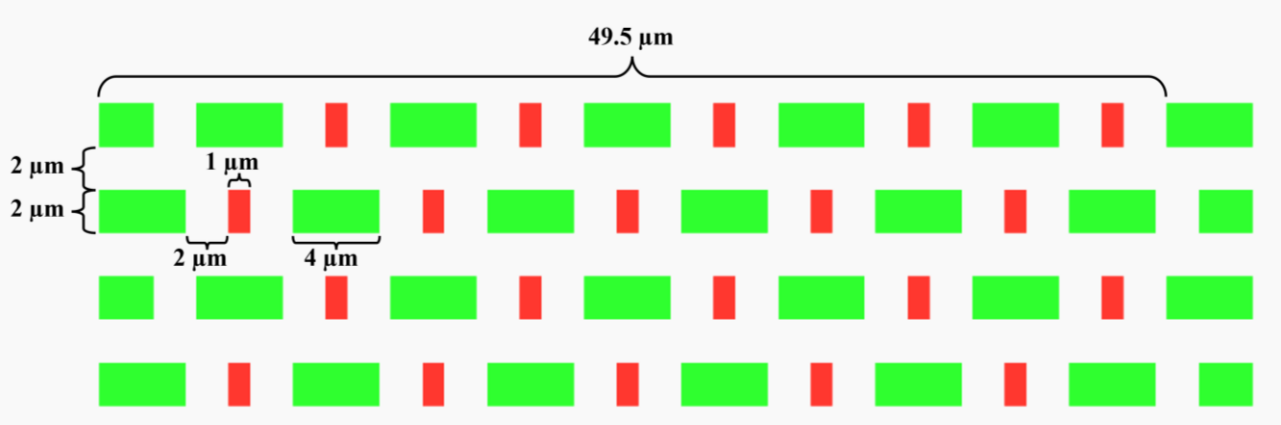
- Channel simulation requires realistic CMOS transmitter model
  - Must capture non-linear effects
- Public IBIS/AMI models not available
  - Created custom parameterized SPICE model
- Matches electrical parameters from UCIe specification
  - Nominal 25Ω output impedance
  - De-emphasis capable, **completely disabled in this work**
- Prevents overly optimistic results compared to an ideal transmitter





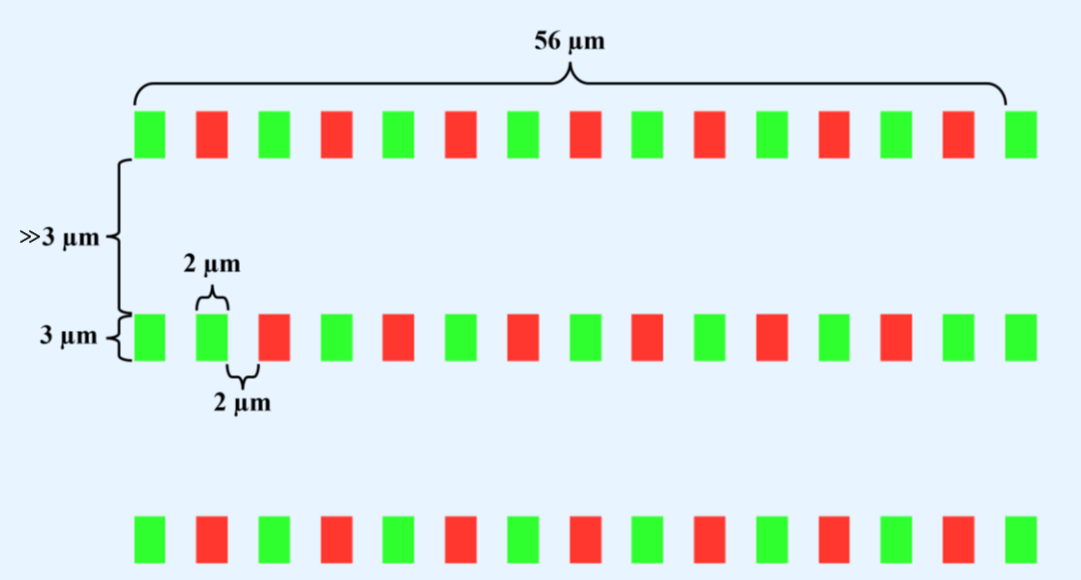


Comparison of Simulation Geometries



Silicon Bridge

- Referenced from literature
- More traditional return path structure
- SiO_2 dielectric, Copper conductor
- VTF Loss/XT matches literature source



Wallstrip

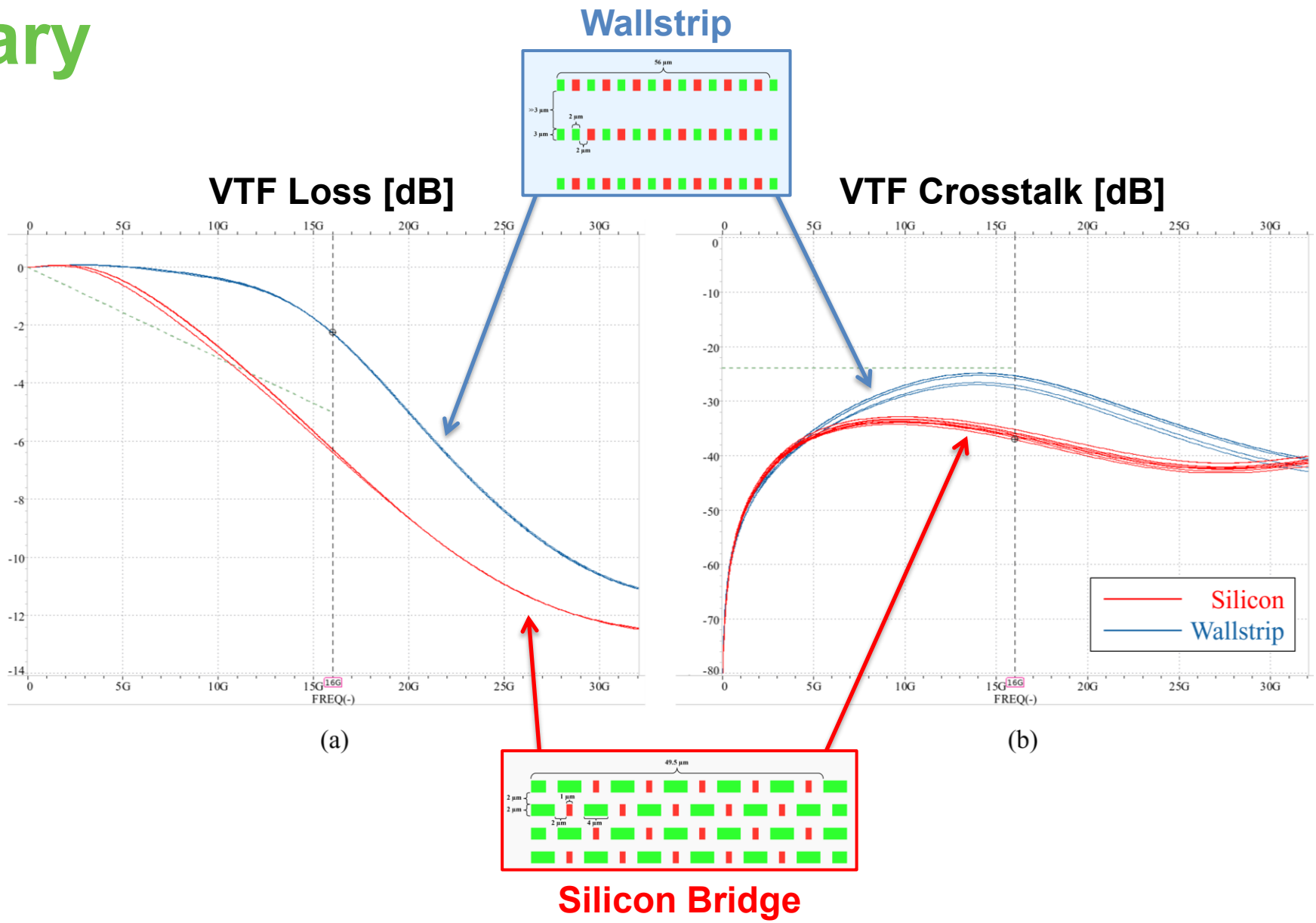
- No planes
- Thicker dielectric/conductor geometry
- Fewer layers
- Organic dielectric, Copper conductor

Results Summary

- Three scenarios investigated:

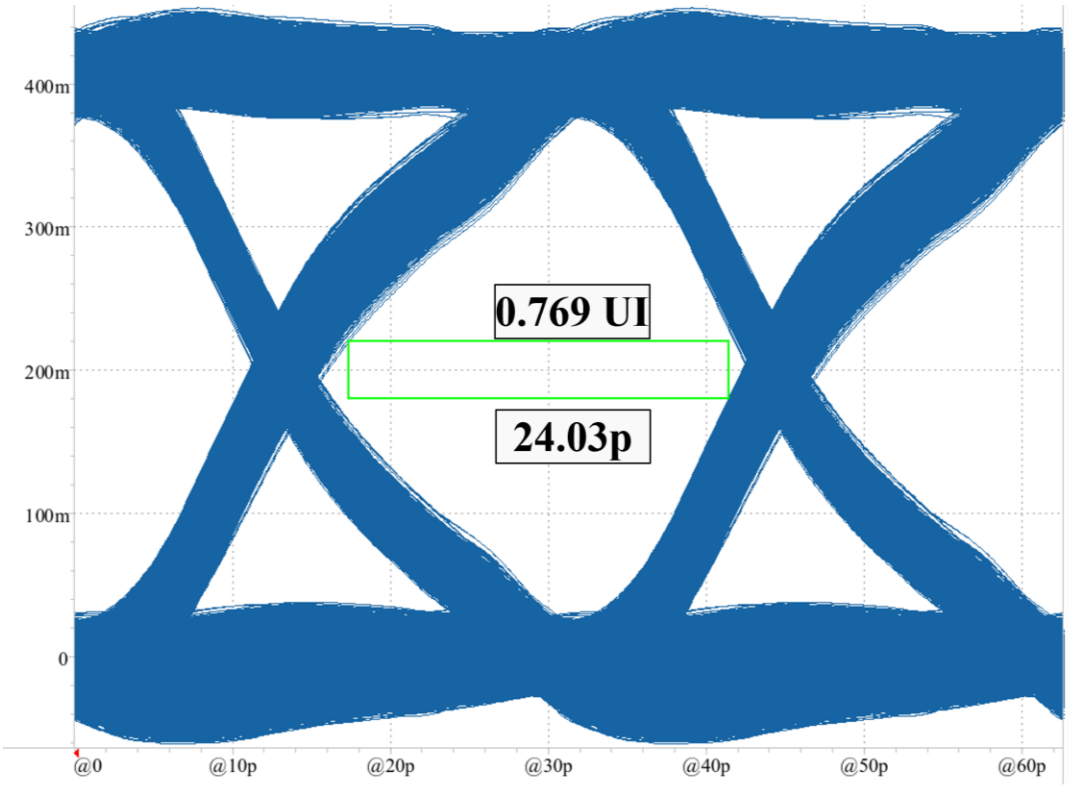
1. 2mm Length, 32 GT/s
2. Maximum routing length at 32 GT/s
3. Maximum data rate at 2mm length

- VTF Comparison at 2mm channel length
  - VTF Loss: Wallstrip
  - VTF XT: Silicon



Scenario 1) 2mm Channel, 32 GT/s

Wallstrip

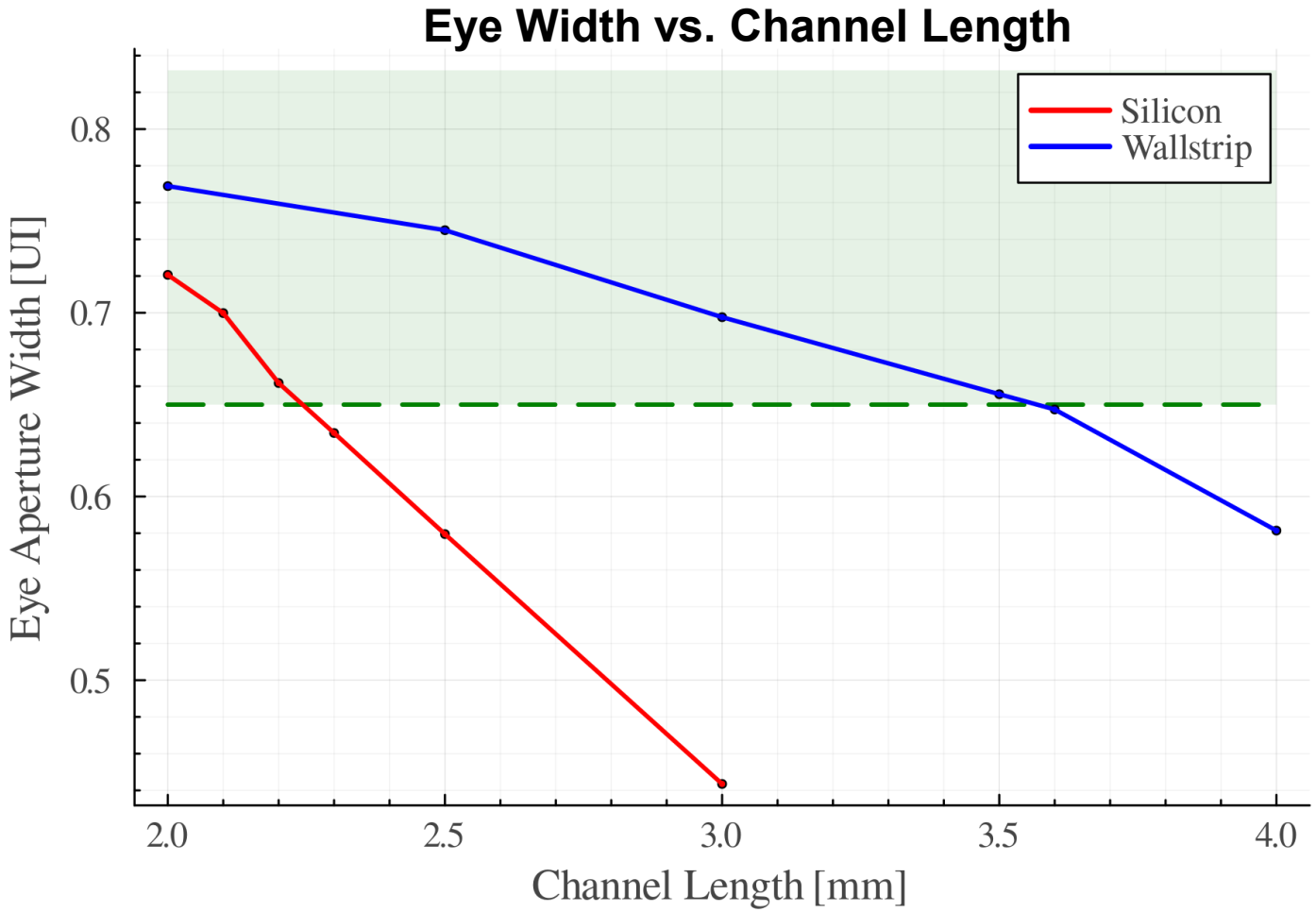


Silicon Bridge

- Wallstrip has more margin to limit than Silicon Bridge

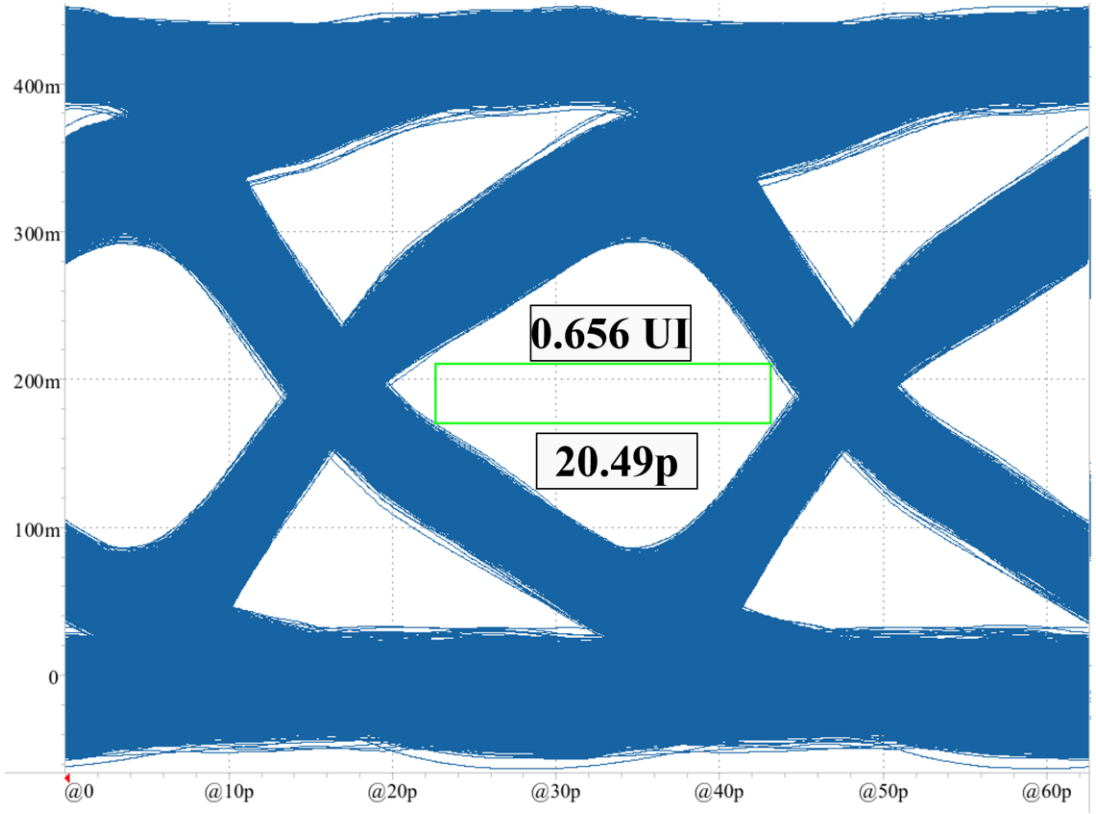
Scenario 2) Channel Length Variation at 32 GT/s

- Plot shows the width of a 40mV rectangular aperture vs. channel length
- Silicon bridge:
  - Passes with 2.2mm max channel length at 32 GT/s
- Wallstrip:
  - Passes with 3.5mm max channel length at 32 GT/s



Scenario 2) Channel Length Variation at 32 GT/s

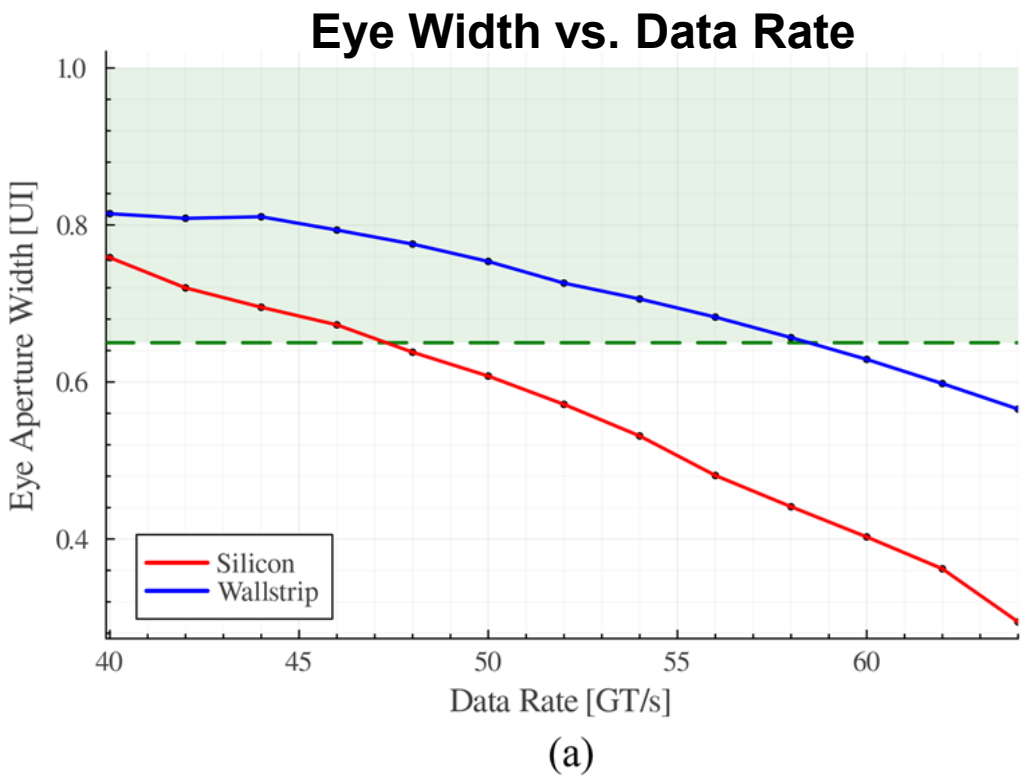
Wallstrip: 3.5mm

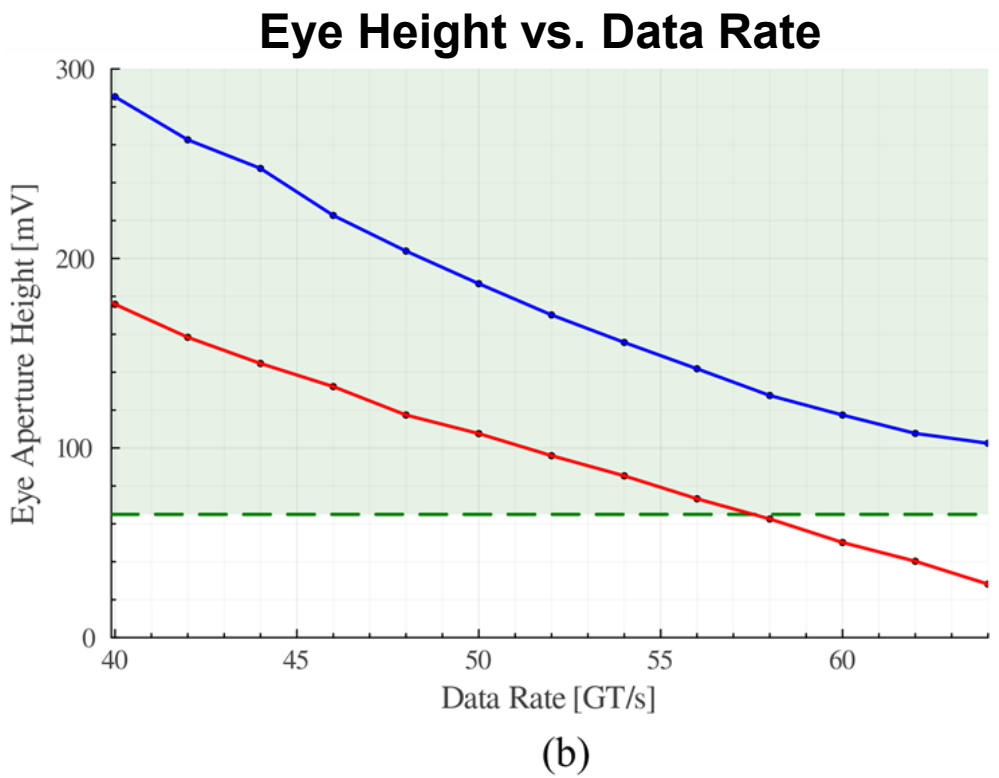


Silicon Bridge: 2.2mm

- 32 GT/s eyes plotted at respective maximum channel lengths

Scenario 3) Data Rate Variation at 2mm Channel

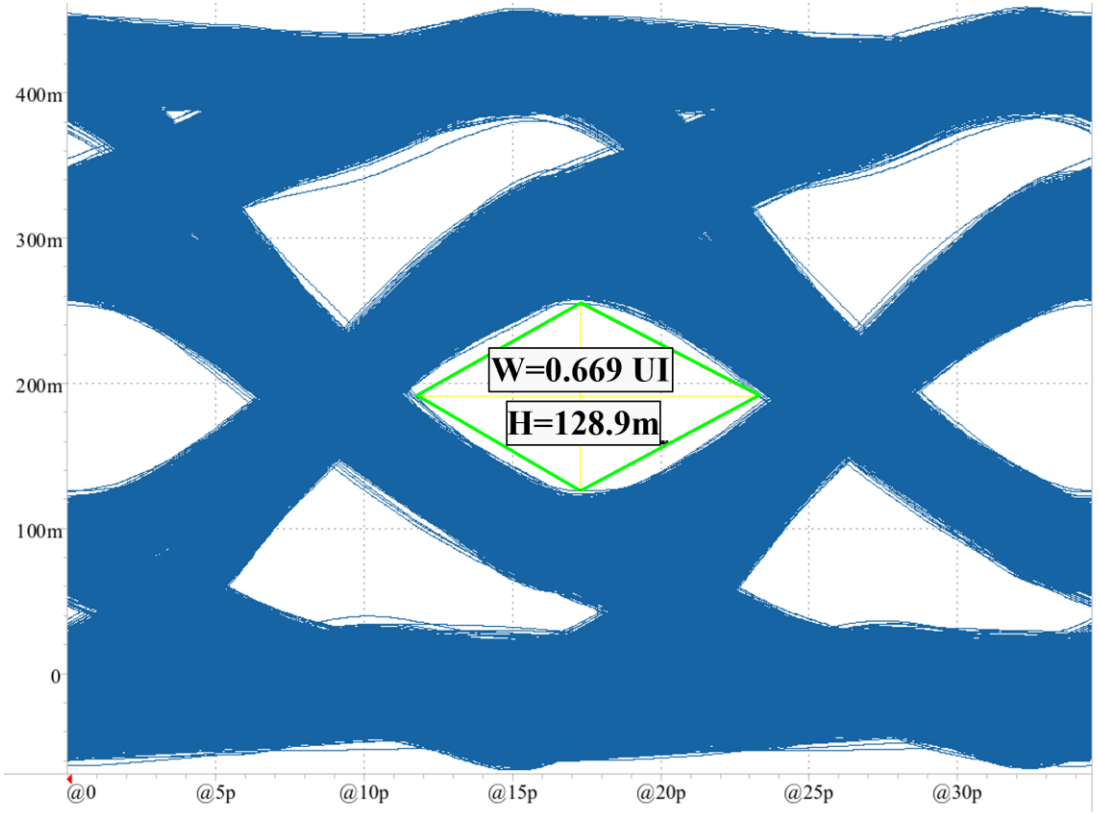




- Plot EW (left) and EH (right) across data rates
- Both Silicon Bridge and Wallstrip are eye width limited
- Silicon Bridge achieves 46 GT/s; Wallstrip can operate at 58 GT/s

Scenario 3) Data Rate Variation at 2mm Channel

Wallstrip: 58 GT/s Preset P0



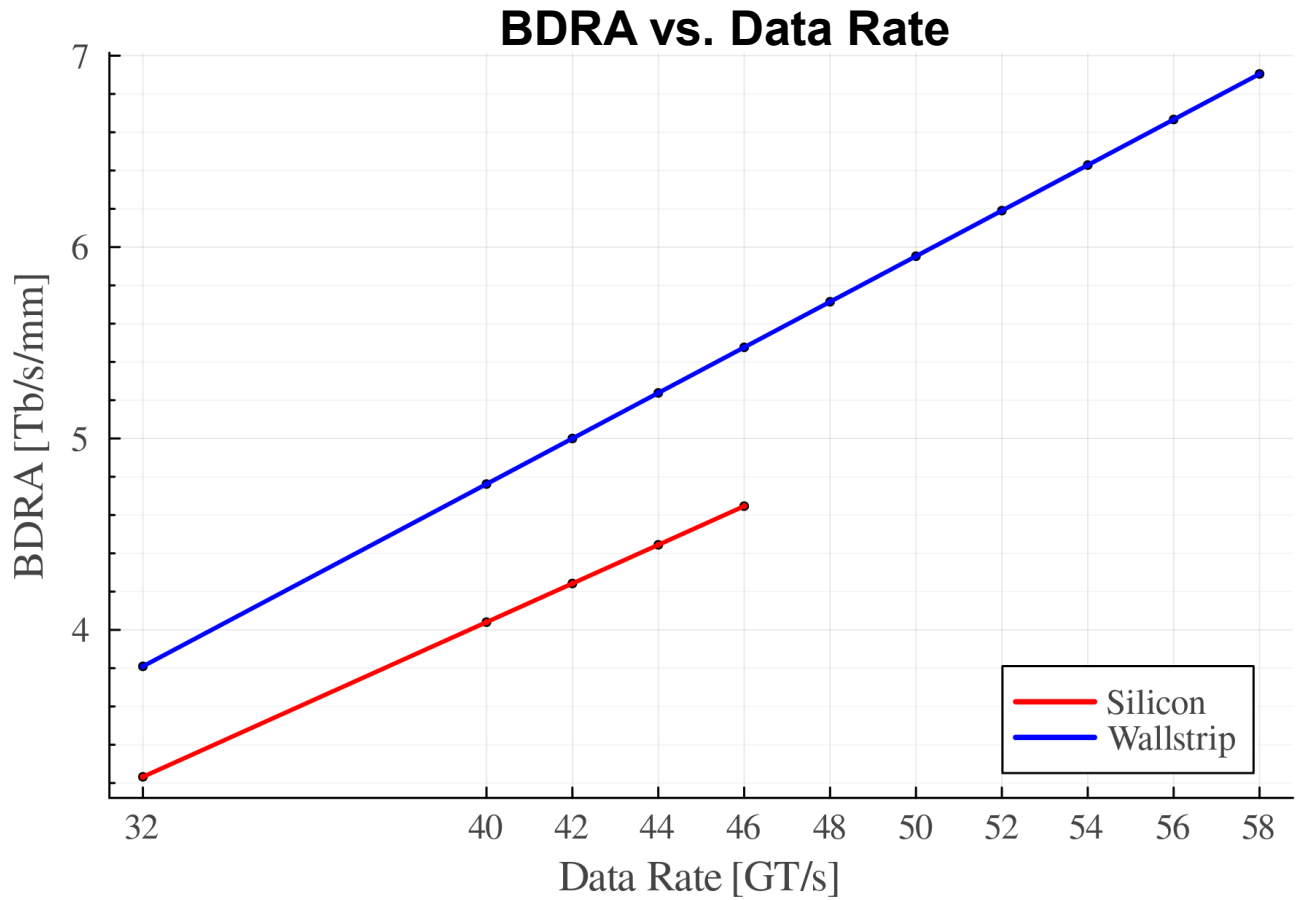
Silicon Bridge: 46 GT/s Preset P0

- Eyes plotted at respective maximum data rates with 2mm channel length
  - Equalization is NOT used

Bandwidth Density per Routing Area (BDRA)

$$\text{BDRA} = \frac{\text{Data Rate [bits/s]} \times \text{Signal Count}}{\text{Routing Width [mm]} \times \text{Layer Count}}.$$

- Bandwidth density traditionally focuses on die shoreline width
- Substrate routing cost is driven by layer count
- BDRA is defined as total throughput normalized to routing area
  - Accounts not only for shoreline width but routing layer count
- Wallstrip significantly boosts BDRA compared to silicon bridge by:
  - Easily supporting higher data rates
  - Requiring fewer routing layers



MORE INFORMATION

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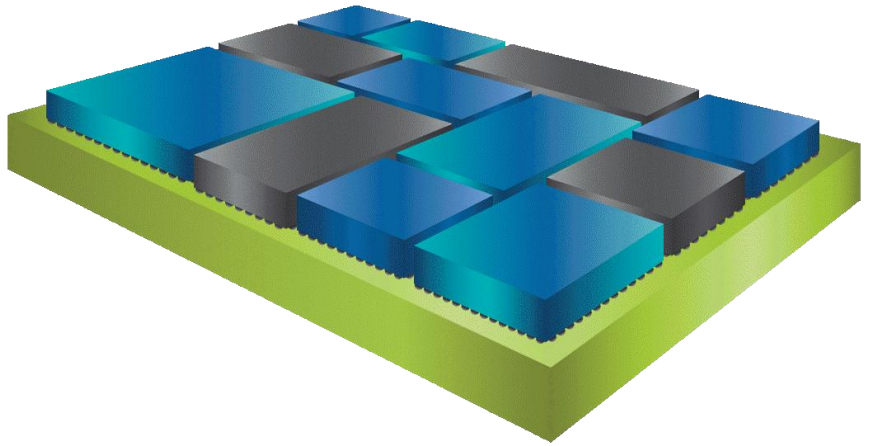

Thank you!

QUESTIONS?